ADVANCED DIELECTRICS FOR GALLIUM NITRIDE POWER ELECTRONICS

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ADVANCED DIELECTRICS FOR GALLIUM NITRIDE POWER ELECTRONICS

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This dissertation details the synthesis, characterization, and application of low-pressure chemical vapor deposited (LPCVD) Aluminum Silicon Nitride ($Al_xSi_yN_z$) dielectrics to AlGaN/GaN based high electron mobility transistors (HEMTs). A detailed study of the effect on A fabrication process for such devices utilizing the $Al_xSi_yN_z$ passivation is presented, and their performance at frequencies ranging from DC to the microwave is compared to devices utilizing more traditional Si_yN_z films for the same purpose.

As AlGaN/GaN HEMT technology has matured, much focus has been placed on the passivation dielectric itself, as many parasitic device mechanisms are directly influenced by it. Metrics such as breakdown voltage, efficiency, and high-frequency dispersion are all greatly affected by the type of passivation applied.

In this work the application of LPCVD $Al_xSi_yN_z$ films as AlGaN/GaN HEMT passivants is presented and shown to yield superior devices to ones passivated with similarly deposited Si_yN_z dielectrics. Breakdown voltage, power added efficiency (PAE), output power density were all measured to be superior on the $Al_xSi_yN_z$ passivated devices when measured under large-signal conditions at 10 GHz.

BIOGRAPHICAL SKETCH

Richard James Brown was born in Greenfield, Massachusetts on April 15, 1982 to Bruce and Catherine Brown (Siano). He attended elementary, middle, and high school in the Greenfield public school system, graduating with a diploma from Greenfield High School in the year 2000. He received the Bachelor of Science, and Master of Science in Electrical and Computer Engineering from Cornell University in years 2004 and 2007, respectively. Since then he has been under the guidance of Professor James Richard Shealy of the department of Electrical and Computer Engineering at the same institution in pursuit of the degree of Doctor of Philosophy.

Dedicated to my father, Bruce Brown, for sparking my interest in figuring out how things work – Something which the completion of this dissertation would have been impossible without.

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CHAPTER 1

INTRODUCTION

1.1 AlGaN/GaN Based Heterojunctions

Semiconductor systems taking on the wurtzite crystal structure possess a unique axis along the [0001] direction, resulting in a macroscopic polarization along this direction for compound semiconductors comprised of atoms of differing valence, such as the AlGaN material system [1,2]. Due to the fact that the polarization is stronger in AlGaN alloys than pure GaN, a AlGaN/GaN heterostructure will evolve a high-concentration two-dimensional electron gas (2DEG) at the material interface as a result of the polarization discontinuity [1]. This allows for the creation of a conduction channel suitable for field effect transistors without the use of barrier doping as is used in other common material systems such as AlGaAs.

1.1.1 Two-Dimensional Electron Gasses in AlGaN/GaN Heterostructures

Depicted in Figure 1.1 is a cross-sectional view of a typical AlGaN/GaN heterostructure grown on a SiC substrate with an AlN sub-buffer layer. Aside from the substrate and AlN layer, a simple structure mainly consists of a thick (~1 μm) GaN buffer layer, capped with a thin (~25 nm) AlGaN layer. Previous calculations and experiments have shown that the spontaneous polarization of AlGaN alloys is stronger compared to that of pure GaN [1,2]. Additionally, the pseu-

domorphic growth of AlGaN directly on top of GaN results in tensile strain in the AlGaN layer, which has a smaller lattice constant than GaN in the basal plane. Applying tensile strain to the AlGaN layer results in an additional piezoelectric polarization that adds constructively to the spontaneous polarization in this layer. Due to the thickness of the GaN layer, it is assumed to be fully relaxed [1,2], hence the polarization in this layer has only a spontaneous component. Figure 1.1 indicates the polarization and electric field components of the AlGaN and GaN layers, as well as the surface and interface charges which result, while Figure 1.2 depicts the corresponding conduction band profile. As the magnitude of the polarization in the AlGaN layer is greater than that in the GaN layer, a net-positive interface charge at the heterointerface equal to the divergence of the polarization results at the heterointerface. To first approximation, the mobile 2DEG density can be estimated to be equal to the discussed positive interface charge, however this does not account for the charge state of the surface or backside of the structure, which cannot be assumed to be equal and opposite the polarization charge densities at these surfaces. It will be shown in Chapter 3 that the charge state on the surface of the structure has a strong influence on the measured heterostructure 2DEG density. Figure 1.3 depicts an actual measurement of the 2DEG density profile with increasing depth into the AlGaN/GaN structure made by the Hg-probe contacted capacitance-voltage (C-V) technique, which will be discussed in more detail in Chapter 3.

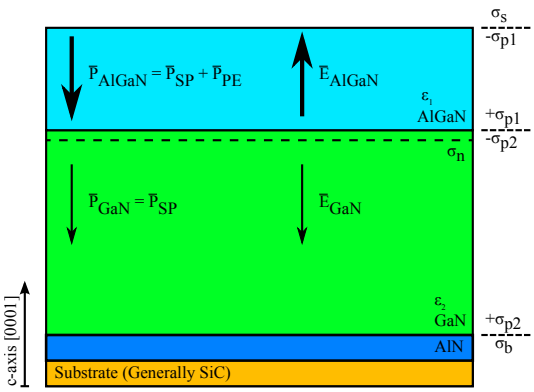

Figure 1.1: Typical cross-section for an AlGaN/GaN heterostructure indicating the material polarization for both layers, the fixed surface and interface charges, as well as the mobile 2DEG that results.

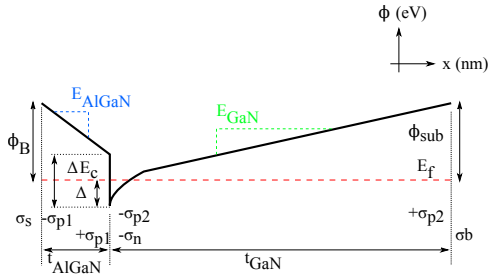

Figure 1.2: Conduction band profile for a typical AlGaN/GaN heterostructure (neglecting the substrate and nucleation layer).

1.2 AlGaN/GaN Based High Electron Mobility Transistors

The first AlGaN/GaN high electron mobility transistor was reported in literature in 1993 [3], quickly following successful metal-organic chemical vapor deposition of high quality single-crystal GaN films on Al_2O_3 substrates [3,4]. Since then, the development of this material system and high electron mobility transistors realized in it has progressed at a rapid pace, with high power density devices operating from DC to the V band [5–20]. The wide bandgaps possible in the AlGaN system, ranging from 3.4-6.2 eV, allow for devices with unprecedented breakdown voltages and operating temperatures [21]. HEMTs realized

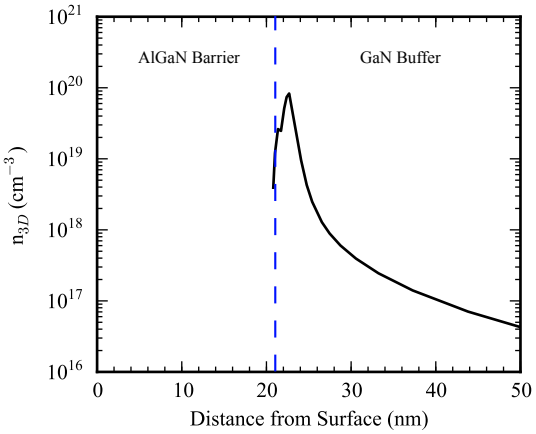

Figure 1.3: The 3-dimensional electron density of a typical AlGaN/GaN heterostructure with a thick (~1 μm) GaN buffer and thin (~25 nm) AlGaN (25% Al) barrier obtained by Hg-probe C-V profiling.

in the AlGaN/GaN system have a 2DEG channel density over 10^{13} cm^{-2}, 10 x higher than what is found in other semiconductor systems, allowing increased current densities on the same order. The breakdown field of the AlGaN/GaN system is >3 MV/cm [22], which is over 3 x that of GaAs or Si [21]. Mobility in the 2DEG of the AlGaN/GaN heterostructure is generally ~1500 cm^{2}V^{-1}s^{-1} and the saturation velocity is on the order of 2 x 10^7 cm/s, giving rise to transistors with high values of unity current gain cutoff frequency (f_T) and maximum frequency of oscillation (f_{MAX}) [23]. The high 2DEG density combined with the high f_T and f_{MAX} and high breakdown field, allows for HEMTs to be driven at high drain bias and current density at microwave frequencies [12,16,22].

1.3 Current Challenges in AlGaN/GaN High Electron Mobility Transistor Development

While the AlGaN/GaN material system does have many superior properties compared to other semiconductor systems which make it ideally poised for the realization of high-frequency high-power transistors, many problems which have proven to be a severe limitation to their adoption have been identified.

1.3.1 DC-to-RF Dispersion

One of the earliest identified and most limiting problems encountered in AlGaN/GaN HEMTs was the so-called "DC-to-RF" dispersion, or microwave "current-collapse," which results in a reduced measured microwave output power compared to the theoretically calculated output power from DC load-line analysis [13,24,25]. In AlGaN/GaN HEMTs without a passivation layer, the AlGaN surface is exposed to the environment where dangling surface bonds are free to absorb ionic charges from atmospheric sources, or when the device is biased, electrons injected from the drain. Due to the fact that the mobile 2DEG charge in the AlGaN/GaN heterostructure evolves as a result in the polarization discontinuity between the AlGaN and GaN layers, and the fact that the AlGaN layer is generally very thin (~20 nm), the 2DEG charge is placed very close to the free surface of the AlGaN, making it sensitive to the charge state that exists there [1,2,26]. For instance, the negative induced polarization charge existing on the surface has been predicted and observed to be able to completely suppress the 2DEG charge in AlGaN/GaN structures with very thin barriers [27].

Also, measurements of the electron and ion lifetimes in trapping states at the free AlGaN surface were measured to be from milliseconds up to several seconds [25]. Slowly trapping and detrapping electrons at the AlGaN surface are widely viewed as being responsible for the observed microwave current slump in unpassivated devices. The trapped electrons serve as "virtual-gates" which allow local modulation of the charge on the AlGaN surface which corresponds to a modulation of charge in the 2DEG. The time constant of these trapping events is on a slower timescale than the applied microwave signals, hence it results in a reduction of the microwave output power.

Since the realization that passivation of the AlGaN transistor post-fabrication with a layer of plasma enhanced Si_yN_z can dramatically reduce the DC-to-RF dispersion effects [24], many different types of insulators deposited by PECVD [8,28–30], MBE [31–40], LPCVD [7,41–43], and ALD [28,31,37,40,44–49] have been investigated as device passivations. However, by far the most popular passivation for these devices remains the PECVD Si_yN_z passivation, as the processing complication added by utilizing it is minimized since it can be applied after the active device is fabricated. The applied passivation serves to tie up the dangling surface bonds at the AlGaN surface, preventing electrons from the drain from occupying the surface states associated with them. With the trapping and detrapping mechanism largely eliminated, the microwave power output of the device can be measured much closer to the value predicted from the DC loadline analysis. It has been shown however that passivation of the HEMT with Si_yN_z does considerably increase the gate leakage measured on the device [50], which is of concern to certain applications requiring low power consumption.

In general LPCVD passivations are viewed as higher quality than PECVD variants due to the high temperature nature of the deposition. LPCVD Si_yN_z has also been shown to not only tie up the surface states of the AlGaN [43], but it has been shown to increase the 2DEG concentration of the structure considerably [27]. This has been shown (and will be discussed in greater detail in Chapter 3) to be due to the provision of fixed positive charge at the insulator/AlGaN interface that serves to cancel the negative induced polarization charge that exists there. However, as will be discussed in Chapter 4, increasing the already large 2DEG density in an unpassivated structure via passivation can lead to the increase in electric field strengths between biased terminals of a HEMT. This leads to lower breakdown voltages and increased dispersion due to high electric fields and hot electron injection on the surface from the drain terminal. A recent HEMT study utilizing LPCVD deposited $Al_xSi_yN_z$ films has shown both excellent mitigation of DC-to-RF dispersion at both 10 and 35 GHz as well as devices with high breakdown voltages [51]. As will be detailed in Chapter 3, this is accomplished by the ability of the LPCVD $Al_xSi_yN_z$ to both tie up the surface states of the AlGaN and add less positive charge to the surface than LPCVD Si_yN_z films; this yields a comparatively lower density 2DEG that reduces the interterminal electric fields in the device. The LPCVD deposition process does however have disadvantages compared to the PECVD one; mainly that it must be deposited prior to any metal deposition steps due to the high-temperature nature of the process. Hence instead of first fabricating the active device and then applying a low-temperature passivation, one must first passivate the heterostructure and then etch through the dielectric to make contact to the AlGaN. The necessity of etching the dielectric has potential implications as far as inducing damage in the AlGaN layer, especially in the gate region. A process to

accomplish this is explained in detail in Chapter 4 of this work.

1.3.2 Management of Electric Fields

As discussed, the AlGaN/GaN heterostructure has a very large 2DEG concentration and a very thin AlGaN barrier. The combination of these leads to very high electric fields between regions of high bias in the device. This problem is in general exacerbated in the case of a passivated structure, as the passivation serves to increase the 2DEG concentration.

While the breakdown field of the AlGaN system is large, device output power is still limitted by the tendency for breakdown on the drain side of the gate [22]. A popular method of reducing the electric fields in this region is the use of a source or gate connected field plate placed between the gate and drain [52–56]. Such structures serve to reduce the charge, and hence the electric field in the gate region, allowing the drain to be biased to a higher voltage and realize higher device output densities. However, this type of electric field reduction comes at the penalty increased parasitic capacitance from the extra metallization which limits the use of such technologies to the lower frequency microwave bands.

Longitudinal electric fields in the source-gate, and gate-drain region arising from the injection of high current densities in the device channel can increase the source and drain access resistances. It has been shown that the measured source access resistance can exhibit a nonlinear increase with increased drain current density [57], which causes a drop in device efficiency and power density. Reducing the fields in these regions by decreasing the electron density in the

channel would be of interest. As the $Al_xSi_yN_z$ passivation has been shown to decrease the 2DEG density in the device channel [51], the interterminal electric fields are similarly reduced.

Ideally, there would be a way to selectively reduce the charge in the channel without the use of a metallic field plate, as this would avoid the penalty of increased capacitance. As will be further detailed in Chapter 3, and as published in literature [51], the use of $Al_xSi_yN_z$ passivations can be successfully used to accomplish this task.

1.3.3 Ohmic Contacts to the AlGaN/GaN System

Ohmic contacts to the 2DEG of the AlGaN/GaN heterostructure have been a challenge to HEMT design since the first studies of such structures. The wide bangap properties of the material make forming a reliable ohmic contact with a simple metallization very difficult, and HEMTs realized in this material system can have access resistances orders of magnitude larger than corresponding contacts in other common semiconductor systems.

Generally, making a contact with a voltage independent resistance to a semiconductor either requires the metal-semiconductor barrier height to be small so that electrons can easily surmount the potential difference, or the barrier itself must be thin enough so that tunneling readily occurs. To first approximation, the barrier height for electrons at a metal semiconductor junction is given by the well known relation in Equation 1.1.

$$\phi_b = \phi_m - \chi_S \tag{1.1}$$

As the electron affinity of the $Al_xGa_{1-x}N$ system has been measured experimen-

tally in a range of 3.25-0.25 eV for values of x from 0-1 by ultraviolet photoelectron spectroscopy [58], making a metal-semiconductor contact with a small potential barrier to AlGaN requires the use of a metal with a correspondingly low work function. The work function of most metals generally exceeds the value of the AlGaN electron affinity by at least 1 eV, with the exception of the environmentally unstable s-block metals [59]. These s-block metals are however impractical to use from a processing standpoint due to their atmospheric reactivity. Heavily n-type doping a thin AlGaN layer in order to make a tunnel contact to the underlying 2DEG is another viable option, and is a common approach taken in many semiconductor systems when a metal of appropriate work function is not available or is impractical to use [60].

Several studies have been made where the AlGaN layer of a HEMT structure was ion implanted with Si and then annealed at very high temperatures to activate the dopant [61–64]. With a high n-type doping concentration, these studies were able to achieve contacts to the AlGaN/GaN 2DEG without the use high-temperature annealed metals - resulting in smooth contacts. However, all of these schemes involved activating the implanted dopant at excessively high (~1200-1500°C) temperatures, requiring either the use of an AlN capping layer or a high partial pressure of atomic nitrogen supplied by an NH_3 ambient to keep the AlGaN layer from losing nitrogen. These special requirements overly complicate the fabrication of HEMTs, requiring non-standard equipment and possibly subjecting the AlGaN/GaN structure to unneeded high-temperature stress.

Several studies exist where the activation anneal temperature for ohmic contact activation was explored through the use of RIE plasma pre-treatment of the

AlGaN surface prior to metal deposition [65–69]. The most successful of these schemes was one based on the RIE pre-treatment a $SiCl_4$ based plasma [65]. This scheme allowed relatively low activation temperatures in the range of 500-600 °C. Such low processing temperatures were explored realize self-aligned HEMTs by first depositing a T-gate type metallization for the gate and then using it as a mask for the ohmic contact deposition. The overhangs of the T-gate provided separation of the resulting ohmic and gate metals and allowed devices with very short source-gate and gate-drain spacing. The low temperature activation prevented the Schottky metallization for the gate from turning ohmic, a problem which generally precludes the deposition of the gate metal prior to the ohmic source and drain metals. A possible disadvantage of contacts such as these is long-term elevated temperature stability, however studies have shown they are stable on the scale of at least ~1000 hrs at temperatures up to ~500 °C [66].

Experimentally synthesized AlGaN compounds are generally n-type, even without intentional doping, an observation some studies attributed to nitrogen vacancies in the lattice which naturally occur [70,71]. Several ohmic contact schemes to bulk layers of GaN and AlGaN as well as AlGaN/GaN HEMTs have further exploited this n-type doping that nitrogen vacancies impart to the AlGaN system by employing a metallization with a low enthalpy of formation for the corresponding metal nitride. This both thins the barrier and imparts n-type doping by consuming some of the available nitrogen in the layer and the metal contact, "advancing" into the surface of the semiconductor. Both titanium and aluminum have metal nitride complexes that are thermodynamically more stable than that of AlGaN compounds at elevated temperatures and have a lower work function than the corresponding metal. As such, successful ohmic con-

tact metallization schemes consisting of Ti/Al or Al/Ti stacks have been widely reported in literature [72–77]. However, due to the high reactivity of both metals, they have a tendency to form resistive and chemically stable oxides which increase their contact resistance with the semiconductor [78]. Studies of stable overlayers for the Ti/Al schemes such as Ti/Au, Ni/Au, and Mo/Au, have been widely reported in literature [14,15,72,79–81], and it is generally claimed that the refractory metal layer Ni, Ti, or Mo serves as to block the diffusion of Au into the Al layer by having a low solid-solubility of Au [82]. As Au and Al have a low temperature eutectic composition, allowing them to come in contact at the high anneal temperatures used for ohmic contact activation can result in lateral flowing of the contact metal, which causes problems in fabricated HEMTs due to the precision of which the source and drain metals must be placed relative to the gate. However TEM studies have shown that there is a complete mixing of all metals used in such schemes, with Au diffusing all the way into the barrier itself [82]. In a study comparing various types of refractory metal barrier layers in the Ti/Al/X/Au system, it was found that Mo produced the smallest degree of lateral flow and the lowest contact resistance compared to other barrier metals explored [82]. Attempts at containing the ohmic metal under a refractory dielectric have been explored with some success [83,84]. However as noted in a recent study, the metallization was seen to expand and crack the dielectric layer, releasing the flowing metal [83]. Further parametric studies of contact stacks and possible metal containment schemes are of interest to further this aspect of AlGaN HEMT technology.

1.4 Layout of this Document

The contents of this thesis are organized into chapters detailing the contributions the work presented has made to the above mentioned challenges in the field of AlGaN/GaN HEMTs. Chapter 2 details the synthesis of novel LPCVD passivations consisting of solid solutions of Si_yN_z and Al_xN_z, with the resulting dielectric being referred to as $Al_xSi_yN_z$. In the same chapter, detailed chemical, structural, and optical characterization is performed on these films, investigating the film stoichiometry, hydrogen content, and structural phase. A measure of film quality is also established through the measurement of wet-etch rates in various solutions and comparing them to literature. Chapter 3 details an investigation of the electrostatic properties of the Si_yN_z and $Al_xSi_yN_z$, and their effect on the AlGaN/GaN heterostructure 2DEG concentration. Chapter 4 details the development of a fabrication process for sub-micron AlGaN/GaN HEMTs utilizing the passivations described in Chapter 2 and addresses several fabrication issues created by the high-temperature LPCVD passivation. Detailed in Chapter 5 is the DC, small-signal, and large-signal characterization of HEMTs passivated with both Si_yN_z and $Al_xSi_yN_z$. Several performance metrics are evaluated and their connection to the passivation type is explored. Chapter 6 discusses work addressing several problems with the ohmic contact technology currently available for the AlGaN/GaN system, presenting a parametric study of V-Group first layer modifications to the traditional Ti/Al/Mo/Au metallization, as well as a look at alternative top-layer metallizations other than Au. Chapter 7 concludes this document and suggests future directions for the studies presented.

CHAPTER 2

DIELECTRIC SYNTHESIS AND CHARACTERIZATION

2.1 Introduction

Deposition of LPCVD silicon nitride has been widely reported utilizing high-temperature (>650°C) decomposition of SiH_2Cl_2 and NH_3 at low pressure (0.1 - 5 Torr) in a sealed hot-wall reaction cell [85–90]. Atmospheric pressure chemical vapor deposition (APCVD) has been reported utilizing a similar apparatus, but with SiH_4 as the silicon precursor and deposition taking place at a higher pressure [89,91]. APCVD is considered inferior to LPCVD due to the low diffusivity of the reagents at high pressure, leading to nonuniform film compositions and growth rates across samples [92]. Deposition of aluminum nitride has been previously reported by LPCVD utilizing $AlCl_3$ and NH_3 for the aluminum and nitrogen precursors [93], and by low-pressure catalyzed CVD utilizing trimethylaluminum (TMAl) and NH_3 precursors [94]. These studies suggest the addition of a TMAl flow to the SiH_2Cl_2 and NH_3 flows in a LPCVD silicon nitride growth system is a reasonable method of growing of an aluminum nitride / silicon nitride thin film alloy. This chapter details the apparatus and method of synthesizing dielectrics which are made up of a solid solution of Si_yN_z and Al_xN_z as well as the characterization of the film's structural, physical, and chemical properties.

2.2 Experiment

Thin films of Si_yN_z, Al_xN_z, and their alloys, ranging in thickness from 30-75 nm were deposited on Si samples by LPCVD and used to determine the growth rates, composition, and optical properties of the films.

2.2.1 Film Growth Apparatus

All films in this study were deposited by LPCVD in a system schematically depicted in Figure 2.1. The reaction chamber consists of a resistively heated hot-wall quartz cell operated at low pressure. A graphite susceptor was used to hold the substrates in the middle of the tube for deposition with the surfaces of the samples parallel to the direction of gas flow. CVD growth in low pressure has been shown to be important to realizing uniform growth across multiple samples in such systems [92], hence depositions were carried out at a pressure of 2 Torr. Temperatures spanning 550°C-750°C were used to determine the growth rate dependence for the chemistries studied. The reactor has 2 gas sources delivered to the tube via nitrogen carrier gas: dichlorosilane (SiH_2Cl_2) for the silicon source, and ammonia (NH_3) for the nitrogen source. Nitrogen was passed through a trimethylaluminum bubbler to provide the aluminum precursor to the cell. All gas flows were regulated via mass flow controllers and switched in or out of the cell in a vent-run configuration. Carrier Gas flows (N_2) for the NH_3 and SiH_2Cl_2 were held constant at a value of 1600 sccm, and the TMAl carrier (N_2) was held constant at a value of 738 sccm. The TMAl bubbler was held at a pressure of 150 Torr, and its enclosure remained at a temperature of ~35°C, giving the TMAl a vapor pressure of 20.52 Torr. The films characterized were

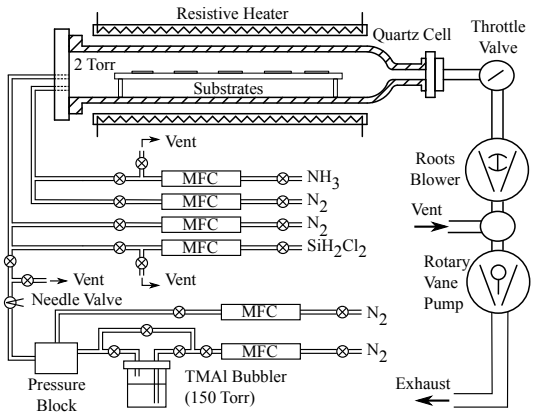

Figure 2.1: Schematic Diagram of the modified ASM deposition system. The tool is set up in a vent-run configuration to allow for the stabilization of precursor gasses prior to their introduction to the process cell. The TMAl bubbler source is held at a pressure 150 Torr while the rest of the system is held at the growth pressure of 2 Torr.

grown on silicon substrates, which were prepared by cleaning in HF, rinsing in DI water, and loaded into the tube immediately thereafter. Gas flow conditions and sample IDs can be found in table 2.1. The aluminum vapor mole fraction (x^v_{Al}) is determined by Equations 2.1 and 2.2: F_{N_2} being the input flow rate of nitrogen to the TMAl bubbler, and F_{TMAl} the equivalent flow rate of TMAl vapor (with vapor pressure VP_{TMAl}) in sccm exiting the bubbler held at an overpressure of P_{Bub}. Equation 2.1 has a 2 in the numerator to reflect that TMAl exists as a dimer [95]. Only F_{TMAl} and $F_{SiH_2Cl_2}$ (flow rate of SiH_2Cl_2 in sccm) are considered in the calculation of the aluminum vapor mole fraction as the NH_3 flow is considered large enough that is it not the limiting reactant.

$$\frac{F_{TMAl}}{F_{N_2}} = \frac{2}{\frac{P_{Bub}}{VP_{TMAl}} - 1} \tag{2.1}$$

Table 2.1: Gas flows used for 5 different film compositions - Silicon nitride, aluminum nitride and 3 different compositions of silicon nitride/aluminum nitride alloy. Growth Temperature for these films was 750°C, and the growth pressure was 2 Torr.

Sample ID #	NH_3 Flow (sccm)	SiH_2Cl_2 Flow (sccm)	TMAl Flow (sccm)	x^v_{Al} (mol. Fraction)
F1 (Si_yN_z)	110	104	0	0
F2 ($Al_xSi_yN_z$)	733	104	3.94	0.024
F3 ($Al_xSi_yN_z$)	733	104	7.47	0.045
F4 ($Al_xSi_yN_z$)	733	104	15.74	0.092

$$x^v_{Al} = \frac{F_{TMAl}}{F_{TMAl} + F_{SiH_2Cl_2}} \tag{2.2}$$

2.2.2 Film Growth Rates

The growth rates of the films were determined through knowledge of the growth time and film thickness measurement by variable angle spectroscopic ellipsometry on a J.A. Woolam Co. VASE instrument. Reported activation energies for the growth of silicon nitride with SiH_2Cl_2 and NH_3 with similar equipment are in the range of ~ 1.5 eV, with growth rates of approximately ~3 nm/min at deposition temperatures near 800°C [90,92,96]. An Arrhenius plot shown in Figure 2.2 illustrates the dependence of the deposition rate vs. inverse temperature for the films grown in this study. The activation energy calculated for the Si_yN_z films in this study was around ~1.3 eV, which compares well with previously reported values [90,92,96]. The activation energies for the $Al_xSi_yN_z$

films were calculated to be ~0.67 eV - much smaller than the Si_yN_z. This smaller activation energy is illustrated in Figure 2.2 by the decreased dependence of growth rate with temperature of these films (which was assumed constant for all values of x^v_{Al}). The activation energy for the growth of Al_xN_z (F5) was the lowest in the study and was calculated to be 0.15 eV. These films showed growth rates of a few nm/min over the entire 550°C-750°C temperature range studied. Figure 2.3 shows the growth rate of the Si_yN_z and $Al_xSi_yN_z$ films as a function of x^v_{Al}; it can be seen that the growth rate of films utilizing both SiH_2Cl_2 and TMAl precursors increases with aluminum vapor mole fraction up to a saturation x^v_{Al} of 0.09. The growth rates obtained for the $Al_xSi_yN_z$ films were ~10x the rate of either the Si_yN_z or Al_xN_z films alone, which is a unique effect not seen in the deposition of other mixed silicon based dielectrics such as SiON, where a monotonic relationship between growth rate and growth vapor mole composition exists [97,98].

2.3 Film Composition

The chemical composition of the films grown in this study were investigated by Rutherford Backscattering Spectroscopy (RBS), Hydrogen Forward Scattering (HFS), X-Ray Photoelectron Spectroscopy (XPS), and Fourier Transform Infared Spectroscopy (FTIR).

RBS measurements are commonly used to determine the stoichiometry of films containing elements with nuclei heavier than Hydrogen [91,99,100]. The technique determines stoichiometry by measuring the energy spectra of high-energy helium nuclei backscattered from the atomic nuclei comprising the film,

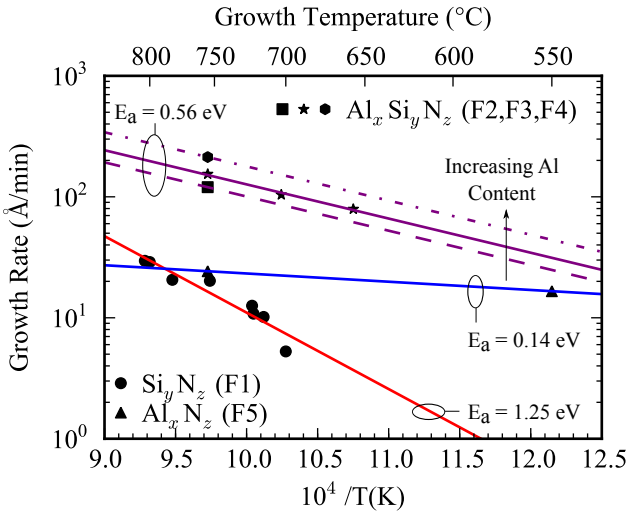

Figure 2.2: Arrhenius plot of growth rate vs. inverse temperature for the films described in table 2.1. The calculated activation energies for the reaction are indicated in the plot. The activation energy for the alloyed $Al_xSi_yN_z$ films was found to be intermediate to those of the Si_yN_z and the Al_xN_z films.

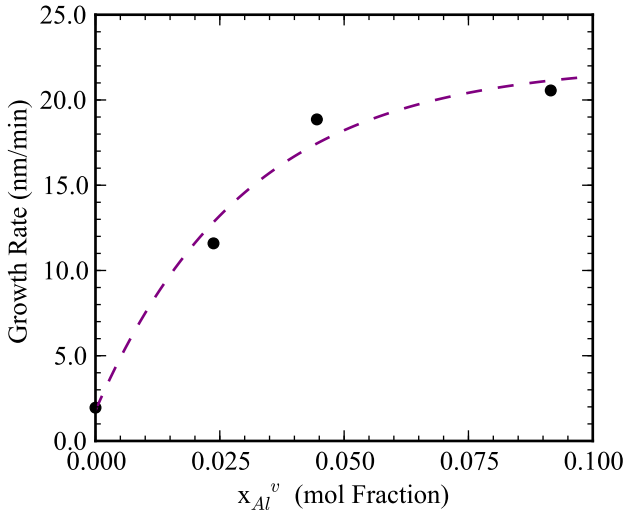

Figure 2.3: Plot of growth rate vs. Al vapor mole fraction. It can be seen that the addition of TMAl flux to the precursors dramatically increases the growth rate and that this increase begins to saturate around an Al vapor mole fraction of 0.25.

making it insensitive to chemical bonding in the film [101]. It has an sensitivity on the order of ~1 at. %, which improves with an increase in the Z-number of the atoms probed. As the RBS technique generally utilizes helium ions as the probe, it cannot detect hydrogen, since it has a negligible backscattering coefficient [101]. To detect hydrogen, the detectors in the RBS setup are angled so as to pick up the forward scattered hydrogen arising from the film with the incoming helium ions at a grazing angle to the film in a measurement known as HFS [101].

XPS measurements are commonly used to determine stoichiometries for thin films similar to the ones investigated in this study [99,102,103]. The technique investigates the spectra of surface emitted x-ray photoelectrons from the film under investigation [104]. Hence unlike RBS, the technique can give information about the chemical bonding of the species present in the film by looking at characteristic shifts in the collected spectra. It has the disadvantage of only being able to probe the surface layer of atoms in a sample, making the results sensitive to surface contamination. For films examined ex-situ to the growth apparatus, Ar ion milling must be used to reduce the signals coming from atmospherically adsorbed oxygen and carbon contamination so that they do not contribute to the spectral shifts used to determine atomic bonding information. However, milling of this type can also sputter non impurity atoms in the film under investigation, affecting the accurate determination of stoichiometry. To determine the stoichiometry of the film only, the milling can be omitted and the impurity peaks detected can just be ignored [104].

FTIR measurements find common use in determining relative hydrogen concentrations in thin films, owing to the large number of detectable phonon res-

onances between hydrogen and other species existing in the infared [105–107]. While the analysis does not provide an absolute measure of hydrogen content, it can be used to monitor the relative concentration in a sample exposed to various processing steps, such as high-temperature annealing [108,109].

2.3.1 Film Stoichiometry: Rutherford Backscattering Measurements

RBS analysis was done at Cornell University utilizing a 2 MeV source of He^{2+} ions with an accumulated charge per sample of 40 μC and a scattering angle of 15.6°. RBS spectra for the Si_yN_z (F1), $Al_xSi_yN_z$ (F4), and Al_xN_z (F5) are shown in Figure 2.4. For the Si_yN_z film, only silicon and nitrogen peaks (along with the silicon substrate background) are present in the spectra - indicating that no other heavy (heavier than hydrogen) impurities are present in the film in a measurable amount. Carbon and oxygen are common impurities found in films of this type [86], but were not detected in this measurement. For the $Al_xSi_yN_z$ film shown, an aluminum peak is present in addition to the silicon and nitrogen peaks, indicating successful aluminum incorporation into the film. For the Al_xN_z film, only aluminum and nitrogen peaks are observed, as expected. The the relative concentrations of the elements present were calculated by fitting simulated to collected RBS spectra using the SIMNRA ion beam analysis package [110]. The results of these fits are collected in Table 2.3, and the relative atomic Al concentration measured in the film is plotted in Figure 2.6 as a function of aluminum vapor mole fraction. As indicated in the table, the Si_yN_z film was measured to be near stoichiometric (Si_3N_4), which which given the growth

Table 2.3: Film composition as calculated from the theoretical fit to the experimental RBS data. The concentrations are in at. %, and relative terms only - as it is known from forward scattering experiments that the Hydrogen content of the film is approximately 3.5%.

Sample ID	Al Content (x)	Si Content (y)	N Content (z)
F1 (Si_yN_z)	-	41.2%	58.7%
F2 ($Al_xSi_yN_z$)	4.4%	36.8%	58.6%
F3 ($Al_xSi_yN_z$)	7.3%	38.2%	54.3%
F4 ($Al_xSi_yN_z$)	13.4%	32.2%	54.2%
F5 (Al_xN_z)	50.7%	-	49.2%

conditions in Table 2.1, agrees with previous studies where films of this type result from NH_3/SiH_2Cl_2 ratios greater than 1 [86,88–90], and silicon-rich films require the ratio to be significantly less than 1 [99]. Also of note in Table 2.3 is the nitrogen/aluminum ratio in the films, where we see that with the increase in film aluminum concentration, a stronger decrease in silicon rather than nitrogen concentration results. This is likely due to the much larger enthalpy of formation of AlN over SiN [111], which results in the aluminum preferentially bonding to the nitrogen.

Film Hydrogen Content: Forward Scattering Measurements

The theoretically calculated fits were done assuming there was no hydrogen in the film, as there is no way for it to be detected in by the RBS (back-scattering) experiment due to its small atomic mass. Instead, the hydrogen content of the films was determined in the same apparatus set up in forward scattering mode, which has been used in previous studies with good results [112,113]. This mea-

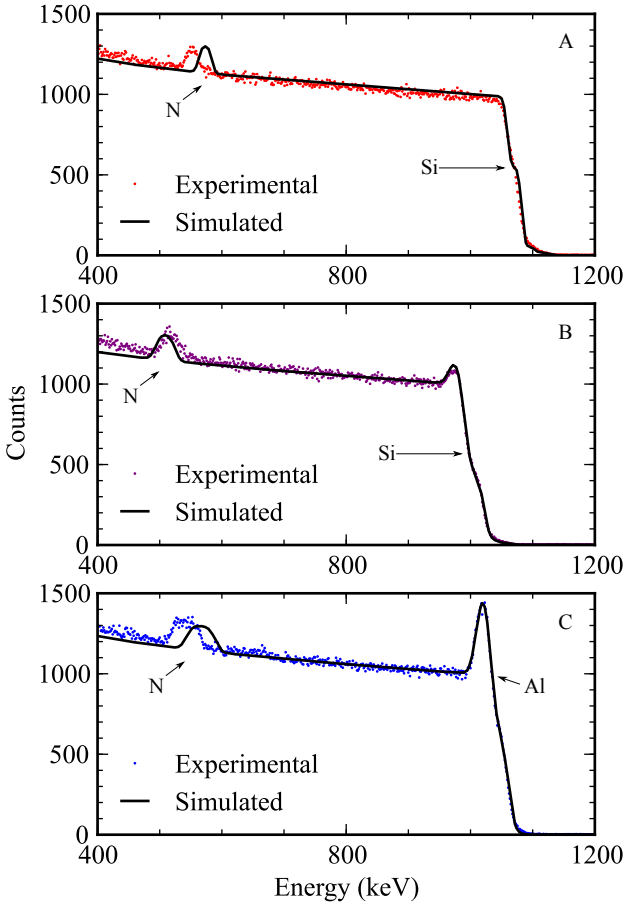

Figure 2.4: Collected RBS Spectra (dots) and theoretical fit (line) for Si_yN_z (A), $Al_xSi_yN_z$ (B) and Al_xN_z (C). Indicated on the plot are the positions for the aluminum, silicon and nitrogen peaks. The baseline of the data is from the substrate and it is taken into account in the theoretical fit. No impurity species were detected in this measurement.

surement was performed on one of the $Al_xSi_yN_z$ (F2) films, and its hydrogen content was found to be about 3.5%. Due to the fact that all the films were grown in the same manner it was assumed they all had a hydrogen content on this same order. As such, Table 2.3 represents the concentration of the elements described in relative terms only.

2.3.2 Film Stoichiometry: X-Ray Photo-Electron Spectroscopy Measurements

XPS measurements were performed at Cornell University on a Surface Science Instruments SSX-100 system, with an aluminum anode source supplying 1486.6 eV X-Rays. The data collected was analyzed using the CASA XPS analysis software suite [114]. Survey spectral scans were performed over a range of binding energies to identify the components present in the film. Figure 2.5 shows a survey scan on an $Al_xSi_yN_z$ (F2) film with the peaks corresponding to atomic species shown and labeled. As can be seen along with the aluminum, silicon, and nitrogen peaks, peaks from carbon and oxygen contamination are also present. These impurity peaks are common features on films examined ex-situ, and arise from atmospheric contamination of the surface [115,116]. The contamination was assumed to only be present on the surface of the films as ion-milling the samples in-situ the XPS apparatus and rescanning was seen to significantly diminish the intensity of the contaminant peaks. The atomic concentrations of the species of interest for all the grown films are compiled in Table 2.4, and the relative aluminum concentration in the film vs. vapor aluminum mole fraction is plotted in Figure 2.6 along with the previously described RBS data. Of note is that the RBS measurements yield a higher ratio of Si/N than the XPS measurements. However this could be due to the fact that the XPS measurement only has access to the surface of the films, which could have slightly different stoichiometry than the bulk. We do however see a constant nitrogen/aluminum ratio in the films - similar to what is seen in the RBS measurements, but more consistent in that the nitrogen concentration does not vary more than 1% across the different Si_yN_z and $Al_xSi_yN_z$ compositions. Detailed peak analyses to quantify how the

Table 2.4: XPS Analysis showing the relative concentrations of aluminum, silicon, and nitrogen in at. % on the surface of the grown films. The Carbon and Oxygen content is ignored, as is the known Hydrogen content measured by forward scattering - only the relative concentrations of the listed species is tabulated.

Sample ID	Al Content (x)	Si Content (y)	N Content (z)
F1 (Si_yN_z)	-	55.6%	44.4%
F2 ($Al_xSi_yN_z$)	5.6%	50.8%	43.5%
F3 ($Al_xSi_yN_z$)	8.8%	47.8%	43.4%
F4 ($Al_xSi_yN_z$)	11.5%	46.4%	42.1%
F5 (Al_xN_z)	60.2%	-	39.8%

different species in the film are bonded by measuring known binding energy peak shifts have been shown possible [99,102,103], but were not utilized due to the large impurity concentration on the surface of the films which resulted in measured binding energy shifts being largely in the direction of the impurity peaks. Since it was determined there was no oxygen in the bulk of the film, the nature of the bulk film bonds could not be extrapolated from this information. Analysis post in-situ surface ion-milling was not utilized, as it has been shown that ion cleaning in this manner can lead to preferential sputtering of the non-impurity atoms - resulting in a false representation of the pre-cleaning stoichiometry, hence this cleaning step was not used for tabulation of any of the data discussed [117].

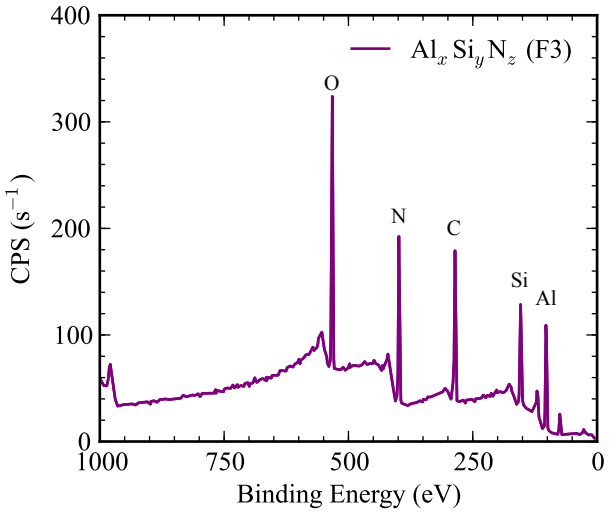

Figure 2.5: XPS survey scan of $Al_xSi_yN_z$ showing the binding energy positions and peaks for aluminum, silicon and nitrogen. The Oxygen and Carbon impurity peaks are due to surface contamination from atmospheric exposure.

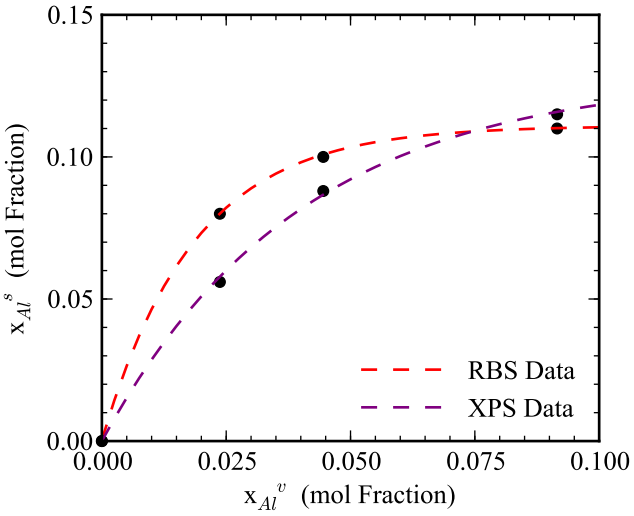

Figure 2.6: Film Al fraction vs. Vapor Al fraction as calculated by both RBS and XPS. Both measurements point to the film Al fraction saturating with added vapor Al fraction, with XPS predicting a sharper transition into the saturation region.

2.3.3 Film Hydrogen Content: Fourier Transform Infared Spectroscopy

FTIR scans of the grown films was performed on a Brukker Optics - Vertex80v Mid-IR system in reflection mode with an angle of incidence of 70°, backed by a gold mirror to increase the optical intensity at the detector. Signature absorption peaks for phonon modes in the Si_yN_z (F1) and $Al_xSi_yN_z$ (F3) films are displayed in Figures 2.7 and 2.8, respectively. Of particular interest were the hydrogen resonances in the film, as hydrogen has been shown to play an important role in the electronic properties of dielectric films used as passivations on semiconductor devices [109,118]. A N-H peak was observed around 3300 cm^{-1}, a Si-H peak around 2400 cm^{-1}, a Si-N double peak identified around 1000 cm^{-1}, and a small H-N-H peak around 1250 cm^{-1}. These peaks were identified by prior work detailing the FTIR of LPCVD [105] and PECVD [106,107,116,119–123] silicon nitride. For the $Al_xSi_yN_z$ spectra, the known Al-N peak from prior work on LPCVD AlN [124] around 690 cm^{-1} is obscured by the large Si-N peak which occupies the same spectral range. The N-H and Si-H Hydrogen resonances can be seen enlarged as inset in the figures.

Post-Growth Annealing and Hydrogen Content

To investigate the effects of post growth annealing on hydrogen content, the films were annealed at 800°C-1000°C for 1 minute in a nitrogen purged rapid thermal annealer (RTA). Figures 2.7 and 2.8 show example scans pre and post annealing and it is noticed that the annealing reduces the N-H and Si-H peaks in the spectra significantly. This observation agrees with similar annealing ex-

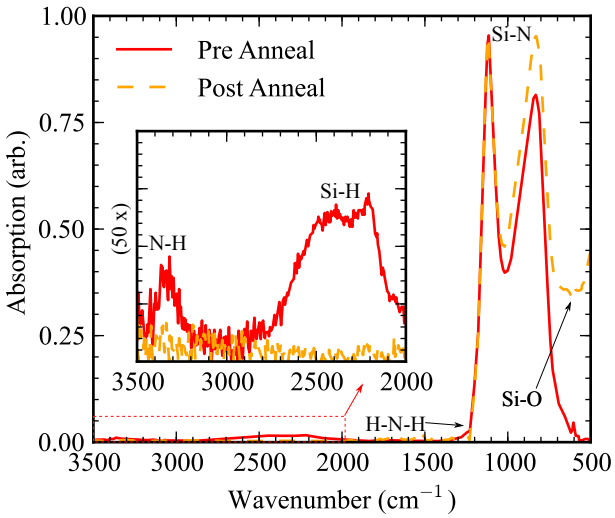

Figure 2.7: FTIR absorption spectra for film F1 - Si_yN_z before and after a 30 second 1000 anneal in N_2. Indicated on the spectra are the positions of phonon modes for the species present in the film. It can be seen that annealing the film significantly reduces the absorption from the N-H and Si-H modes in the 3500 cm^{-1} to 2000 cm^{-1} region.

periments performed on Si_yN_z films in prior work [108,109,125–127]. It is however noticeable that the N-H peak is more difficult to eliminate than the Si-H peak, which also agrees with prior work [116]. Of note is the appearance of a Si-O peak around 500 cm^{-1} post-anneal, this is likely due to moisture or Oxygen contamination in the RTA, as it is not noticed in the as-grown samples. Also of particular interest is the observation that the Si_yN_z film required a 1000°C anneal to significantly reduce the intensity of the Si-H and N-H absorption peaks while the same result was achieved in the $Al_xSi_yN_z$ film at an anneal temperature of only 800°C.

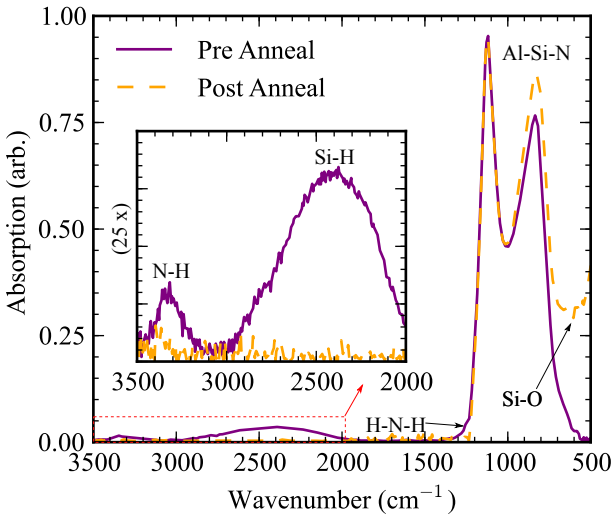

Figure 2.8: FTIR absorption spectra for film F3 - $Al_xSi_yN_z$ before and after a 30 second 800°C anneal in N_2. Indicated on the spectra are the positions of phonon modes for the species present in the film. It can be seen that annealing the film significantly reduces the absorption from the N-H and Si-H modes in the 3500 cm^{-1} to 2000 cm^{-1} region. This reduction occurs at a much lower temperature than the same reduction noted for the Si_yN_z film as plotted in figure 2.7, which required anneal at 1000°C to achieve the same effect.

2.4 Film Optical Properties: Variable Angle Spectroscopic Ellipsometry

For the films described in Table 2.1, film thicknesses and optical constants were determined by VASE on a J.A. Woolam Co. instrument. Figure 2.9 shows the refractive index of the sample films measured in the UV to the Mid IR range. As shown in Figure 2.9, the films grown with a TMAl flow have a lower IR refractive index than ones grown with only silicon and nitrogen precursors. Previous studies of the refractive index of Si_yN_z and Al_xN_z measured infared values of ~2.0 for both films, but due to the band-edge of Al_xN_z being further into the UV,

the visible value of refractive index is consistently lower for the Al_xN_z films. As such, it is expected that a mixed film of silicon nitride and aluminum nitride should posses an index of refraction and band-edge, intermediate of the two individual films. Two identical samples of $Al_xSi_yN_z$ (F3) were also investigated via VASE to see if nitrogen RTA annealing resulted in any measurable change in film thickness or index of refraction. Plotted in Figure 2.10 are the results of this experiment, which show that anneals of 1000°C and 1100°C reduced the thickness of the film by 2.7% and 3.5%, respectively after only 30 seconds of exposure. It can also be seen that further annealing at these temperatures did not further reduce the thickness of the films. We also see in Figure 2.11 that annealing the film at 1000°C for 60 seconds increases the film index of refraction by about 1.25%. Both the thinning of the film and its increase in refractive index upon annealing agree well with previous work [108,125–127], and support the FTIR evidence showing that hydrogen is removed by the anneals. Previous studies have reported that LPCVD Si_xN_y is stable with anneals up to 1100°C, after which nitrogen begins to escape the film [99]; Therefore we can expect that the anneals performed on the samples in this study did not change their stoichiometry other than the removal of the hydrogen as seen in the previous section as well as in the stated previous work.

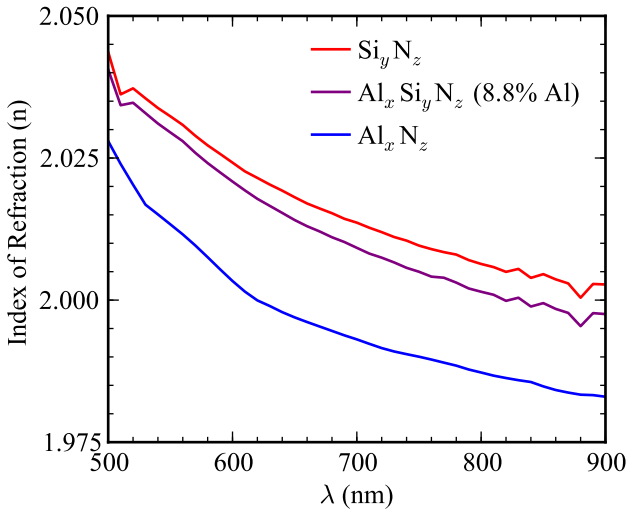

Figure 2.9: Refractive index vs. wavelength for F1 (Si_yN_z), F2 ($Al_xSi_yN_z$), and F5 (Al_xN_z). It can be seen that the $Al_xSi_yN_z$ film has optical properties that fall somewhere between those of Si_yN_z and AlN which would be expected for a composite film of such components.

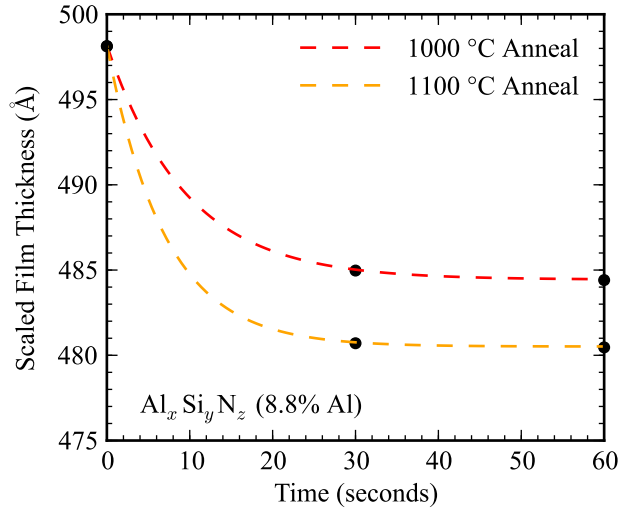

Figure 2.10: Film thickness as measured by spectroscopic ellipsometry of 2 samples of F3 ($Al_xSi_yN_z$) having undergone high temperature nitrogen annealing in an RTA system. It is evident that the annealing reduces the thickness of the film by a measurable (2.7%, and 3.5% of the original thickness for anneals at 1000°C and 1100°C respectively. This is attributed to the reduction of Hydrogen content in the film as observed in 2.8 and 2.7

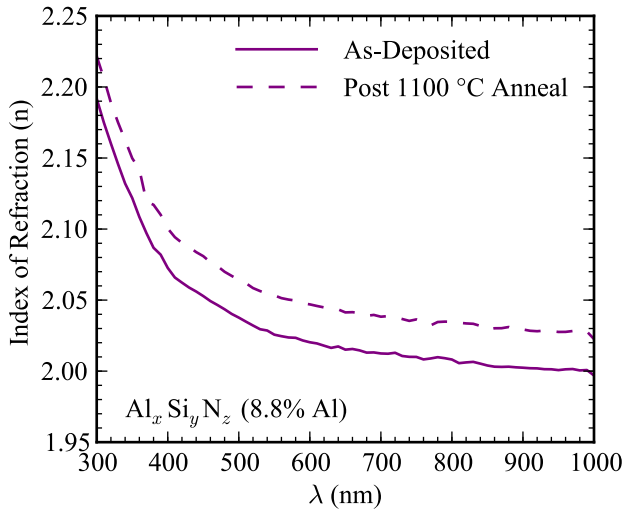

Figure 2.11: Index of refraction for film F3 ($Al_xSi_yN_z$) before and after a 60 second 1000°C anneal. It is evident that annealing the film at high temperature increases its index of refraction at all wavelengths.

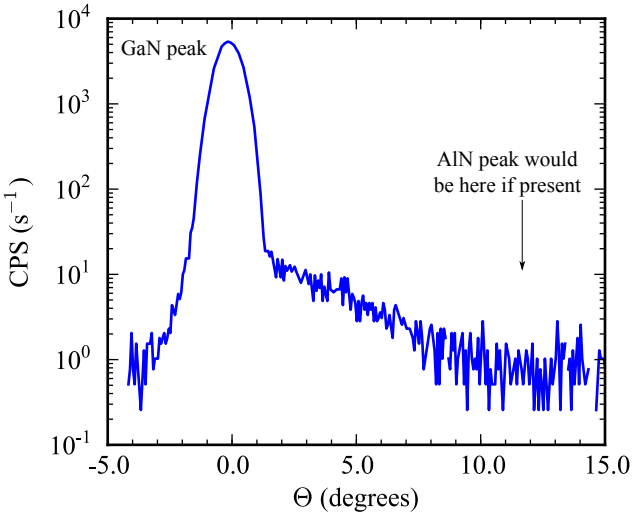

Figure 2.12: HRXRD plot of Al_xN_z film deposited on an AlGaN HEMT heterostructure indicating the expected position of the AlN crystalline peak and the GaN peak from the heterostructure buffer layer. The lack of a defined AlN peak indicates that the deposited Al_xN_z is amorphous.

2.5 Film Quality: Wet Etch Rate and X-Ray Diffraction Analysis

The films etch rates were tested in 49% aqueous HF acid and AZ400K developer. PECVD Silicon nitride is known to have an etch rate of ~100 x LPCVD silicon nitride, which has been previously reported to etch at 1.1 nm/min in 10:1 (49% HF:H_2O) [128]. Also, aluminum nitride of low crystalline quality is known to be etched by AZ400K developer (in which the active ingredient is KOH) [129]. The LPCVD Si_xN_z and $Al_xSi_xN_z$ films all exhibited an etch rate of about 9.5 nm/min +/- 1 nm/min when etched in 49% HF, and a negligibly small etch rate when etched in the AZ400K developer. While the Al_xN_z film exhibited a negligibly small etch rate in 49% HF, but a favorable etch rate of 15 nm/min in the AZ400K developer. The favorable etch rate of the Al_xN_z in the AZ400K was expected as the film was not being grown at a high enough temperature or on a compatible substrate for crystalline material to form. These suspicions were confirmed by high resolution X-Ray diffraction scans of Al_xN_z films deposited on a epitaxial GaN on sapphire sample as shown in Figure 2.12: The plot indicates no diffraction peak other than the GaN peak - indicating no Al_xN_z of any crystalline quality is present in the film.

CHAPTER 3

CAPACITANCE-VOLTAGE CHARACTERIZATION OF SI_YN_Z AND $AL_XSI_YN_Z$ PASSIVATED ALGAN/GAN HETEROSTRUCTURES

3.1 Introduction

In this chapter, Si_yN_z and $Al_xSi_yN_z$ passivated AlGaN/GaN structures with varying dielectric thickness are explored through the use of Capacitance-Voltage and x-ray diffraction measurements to determine the electrostatic effect the passivation imparts to the 2DEG of the heterostructure.

3.2 Theory

The polarization induced electron concentration n_{2D} at the heterointerface of both passivated and unpassivated AlGaN/GaN heterostructures can be estimated to good approximation though the use of classical electrostatics [26]. The following treatment closely follows the theory given by Shealy et. al. [27], and will be used to calculate the fixed charge at the dielectric interface with the AlGaN surface as well as the mobile 2DEG charge at the AlGaN/GaN interface. Referring to Figure 3.1, the conduction band profile for unpassivated case is shown. The subscripts for the sheet charges denote the region of the structure, with region "1" being the AlGaN barrier and region "2" the GaN buffer. The charge densities indicated at the interfaces are as follows: $-\sigma_{p2}$ and $+\sigma_{p2}$ represent the polarization induced sheet charges at the top (AlGaN facing) and bottom (substrate facing) surface of the GaN layer, respectively. It is assumed

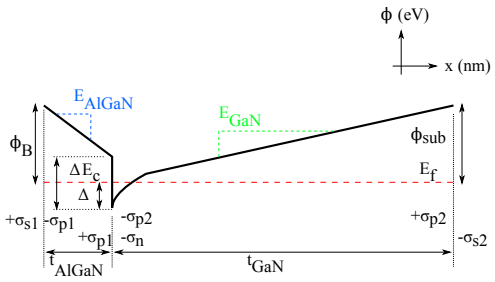

Figure 3.1: Conduction band diagram for both the unpassivated AlGaN/GaN heterostructure.

to have only a spontaneous contribution, as it is grown thick enough to be fully relaxed and have no piezoelectric component of polarization. The sheet charge densities $-\sigma_{p1}$ and $+\sigma_{p1}$ represent the polarization induced sheet charges at the top (free surface facing) and bottom (GaN facing) surface of the AlGaN barrier layer, respectively. σ_{p1} has both a larger spontaneous component than σ_{p2} and a piezoelectric component which adds to the spontaneous due to being coherently strained on the GaN buffer. Hence $(\sigma_{p1}-\sigma_{p2})$ at the AlGaN/GaN interface yields a net positive polarization charge on the AlGaN side of the interface, resulting in a large negative sheet charge σ_n on the GaN side of the interface. The relative permittivies of GaN and AlGaN, are denoted as ε_{GaN} and ε_{AlGaN}, respectively. The slope of the conduction bands indicating the electric fields in the GaN and AlGaN regions are labeled in the figure as E_{AlGaN} and E_{GaN}, respectively. At the AlGaN/GaN interface Gauss' law gives the relation seen in Equation 3.1.

$$\varepsilon_{GaN}E_{GaN} + \varepsilon_{AlGaN}E_{AlGaN} = \sigma_{p1} - \sigma_{p2} - \sigma_n \tag{3.1}$$

with zero field outside the structure equation 3.2 relates the electric field in the barrier layer in terms of the positive surface charge and the AlGaN polarization charge. Assuming zero field outside the buffer similarly yields Equation 3.3. One can then show, by mandating charge neutrality that $\sigma_n = \sigma_{s1} - \sigma_{s2}$; Illustrating the the important impact that the charge state of the structure surface

has on the mobile 2DEG density.

$$-\varepsilon_{AlGaN}E_{AlGaN} = \sigma_{s1} - \sigma_{p1} \tag{3.2}$$

$$-\varepsilon_{GaN}E_{GaN} = \sigma_{p2} - \sigma_{s2} \tag{3.3}$$

Inspecting the band diagram starting at the surface potential ϕ_B, and referencing all energy from the Fermi level (E_f), the relation in Equation 3.4 is derived, where ΔE_c is the conduction band offset at the AlGaN/GaN interface, and Δ is the depth of the quantum well confining the charge.

$$\phi_B - t_{AlGaN}E_{AlGaN} - \triangle E_c + \triangle = 0 \tag{3.4}$$

Assuming all charges occupy the lowest sub-band of the well, Δ can be determined as in Equation 3.3.

$$\Delta = \frac{\pi\hbar^2\sigma_n}{q^2m^*} \tag{3.5}$$

The capacitance per unit area of the GaN and AlGaN layers is given by Equations 3.7 and 3.6, respectively. Equation 3.9 which gives the 2DEG density for the heterostructure, is obtained considering the substrate potential (ϕ_{sub}) and defining the surface potential (ψ) as in Equation 3.8.

$$c_{AlGaN} = \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} \tag{3.6}$$

$$c_{GaN} = \frac{\varepsilon_{GaN}}{t_{GaN}} \tag{3.7}$$

$$\psi = \phi_B - \triangle E_c \tag{3.8}$$

$$\sigma_n = \frac{\sigma_{p1} - \sigma_{p2} - c_{AlGaN}\psi - c_{GaN}\phi_{sub}}{1 + c_{AlGaN}(\frac{\pi\hbar^2}{q^2m^*})} \tag{3.9}$$

This equation simply states that the 2DEG concentration is equal to the polarization discontinuity at the AlGaN/GaN interface minus the depletion from the surface (ψ) and substrate (ϕ_{sub}) potentials.

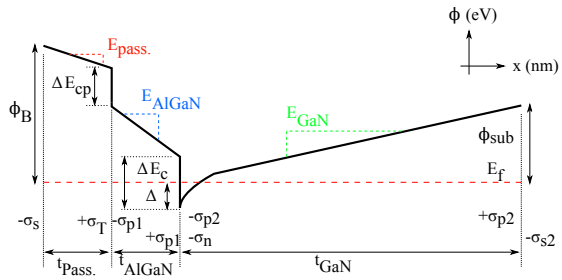

Figure 3.2: Conduction band profile for the passivated AlGaN/GaN heterostructure.

To modify Equation 3.4 to describe the passivated structure shown in Figure 3.2, Gauss' law establishes the new equilibrium at the passivation/AlGaN interface described in Equation 3.10.

$$\phi_B - t_{pass.}E_{pass.} - t_{AlGaN}E_{AlGaN} - \Delta E_{cp} - \Delta E_c + \Delta = 0 \tag{3.10}$$

Where $t_{pass.}$ and $E_{pass.}$ are the dielectric thickness and electric field, respectively of the passivation layer. To modify Equation 3.9, a term to account for possible trapped charge at the passivation/AlGaN interface (σ_T) must now be included in the numerator, and c_{AlGaN} is replaced with c_B; which is a series combination of the dielectric capacitance and the AlGaN barrier capacitance given in Equation 3.11. The last modification to 3.9 is to replace the barrier potential ψ with a new term, $\psi_{pass.}$ which is given in Equation 3.12. The resulting formulation for the 2DEG sheet charge is given by Equation 3.13.

$$\frac{1}{c_B} = \frac{1}{c_{pass.}} + \frac{1}{c_{AlGaN}} \tag{3.11}$$

$$\psi_{pass.} = \phi_B - \Delta E_{cp} - \Delta E_c \tag{3.12}$$

$$\sigma_n = \frac{\sigma_{p1} - \sigma_{p2} - c_B\psi_{pass.} - c_{GaN}\phi_{sub} - \frac{c_B}{c_{pass.}}(\sigma_{p1} - \sigma_T)}{1 + c_{AlGaN}(\frac{\pi\hbar^2}{q^2 m^*})} \tag{3.13}$$

As was assumed in the study by Shealy et. al., the surface ($\psi_{pass.}$) and substrate (ϕ_{sub}) potentials were roughly equal, at a value of ~1.04 eV due to the assumption that the Fermi level in the GaN buffer taking on the value measured from

Table 3.1: Summary of epitaxial material used in this study, indicating barrier thickness, n_{2D}, and the type and thickness of passivation applied.

ID	t_{AlGaN} (nm)	n_{2D} (cm^2)	Passivation	$t_{pass.}$ (nm)
546E1	22.6	1.45 x 10^{13}	Si_yN_z	62.6
546E4	18.7	1.45 x 10^{13}	$Al_xSi_yN_z$	75.5

internal photo-emission studies [130]. It was also assumed that the additional conduction band offset from the passivation must be absorbed by the surface barrier ϕ_B, giving $\psi_{pass.}$ a value of ~1.04 eV as well.

3.3 Sample Preparation

13x13 mm samples of epitaxial material consisting of $Al_{0.30}Ga_{0.70}N/GaN/Al_2O_3$ with 15-25 nm barrier thicknesses were first characterized by C-V to measure the AlGaN barrier thickness and 2DEG concentration. Table 3.1 lists the sample IDs, their as-grown barrier thicknesses and 2DEG concentrations, as well as the passivation type, and thickness of passivation applied. All samples were then cleaned and coated with Si_yN_z or $Al_xSi_yN_z$ passivations as described in Chapter 2.

3.4 C-V Measurements

C-V samples 546E1 and 546E4 were coated (along with Si substrate witnesses) with Si_yN_z and $Al_xSi_yN_z$, respectively. C-V measurements were made with a

mercury probe from the Materials Development Corporation with a high-side contact area of 4.44 cm^2 and a low-side contact with 48.6 times that area, configured in a concentric configuration. The probe was driven by an Agilent E4980A LCR meter measuring at 1 kHz and a DC bias range of -40 to +10 V. C-V data was regarded valid up to a positive bias value where the majority of the voltage is dropped on the front-side contact as discussed in [131]. Calculations of depletion depth (x_d), 3D electron density profile (n_{3D}), and sheet electron concentration (n_{2D}) were then performed utilizing Equations 3.14, 3.15, and 3.16.

$$x_d(V_a) = \frac{\varepsilon A}{C_m(V_a)} \tag{3.14}$$

$$n_{3D}(V_a) = -\frac{C_m^3(V_a)}{q\epsilon_0 \varepsilon A^2 \frac{dC_m(V_a)}{dV_a}} \tag{3.15}$$

$$n_{2D}(V_a) = \int_{V \leq V_{po}}^{V_F} n_{3D}(x_d) dx_d \tag{3.16}$$

Where C_m is the measured capacitance, V_a is the applied bias, A is the area of the inner Hg contact, and ε is the relative permittivity of the of the Insulator/AlGaN/depleted GaN stack. The measurement produces acceptable results by assuming the Si_yN_z and $Al_xSi_yN_z$ passivations have a relative permittivity close to that GaN and AlGaN which is ~9. The dielectric was then sequentially thinned in 10-15 steps by a 6:1 BOE solution till it was completely removed, with C-V scans being taken in between thinnings. Both the Si_yN_z and $Al_xSi_yN_z$ showed etch rates of ~ 1 nm/min in the 6:1 BOE solution. Through knowledge of the barrier thickness and composition prior to dielectric deposition it was possible to estimate the relative permittivity for both the Si_yN_z and $Al_xSi_yN_z$ passivations post deposition. The passivation and barrier layers form a series capacitor where the electrostatic properties of the barrier layer are well known for a given Al fraction as ε=9.7-1.2(x) [2]. Capacitance data were taken at the

positive end of the bias range to bring the 2DEG up as close to the AlGaN barrier as possible. The estimated relative permittivity (ε_r) (at 1 kHz) for Si_yN_z and $Al_xSi_yN_z$ were calculated to be 8.01 and 7.78, respectively. These values are in agreement with measurements in Chapter 2 of the refractive index of Si_yN_z and $Al_xSi_yN_z$, the latter of which measured a smaller value in the infared- indicative of a smaller permittivity.

3.5 Analysis

Plotted in Figure 3.3 shows the results of the measurement of n_{2D} at various dielectric thicknesses for both Si_yN_z and $Al_xSi_yN_z$ passivated samples. The data were normalized to the value of n_{2D} measured after all of the dielectric was stripped, so the plot indicates the degree of increase in n_{2D} provides. The data were fit to equation 3.13 by taking polarization charge values for the $Al_{0.30}Ga_{0.70}N_z$ structures of σ_{p1}=0.056 C/m^2 and σ_{p2}=0.029 C/m^2 and permittivity values of ε_{AlGaN}=9.4 and ε_{GaN}=9.7, as previously published [2], and using σ_T as a fitting parameter. Shealy et. al. noted that the experimental data for Si_yN_z passivated AlGaN/GaN heterostructures were best fit by setting the trapped interface charge σ_T equal and opposite to the negative polarization charge on the AlGaN surface $-\sigma_{p1}$ [27]. While this was found to be (nearly) true for the Si_yN_z passivated AlGaN/GaN structures in this study, a poor fit to the experimental data resulted on the same structures with the $Al_xSi_yN_z$ passivation. The best fit to the experimental data for the $Al_xSi_yN_z$ passivated structure was achieved with a value of σ_T=0.955σ_{p1}, indicating a remaining fixed negative sheet charge ~1.57 x 10^{12}cm^{-2}. The Si_yN_z passivated sample was best fit with a value of σ_T=1.011σ_{p1}, hence the Si_yN_z passivation slightly more than compensated for

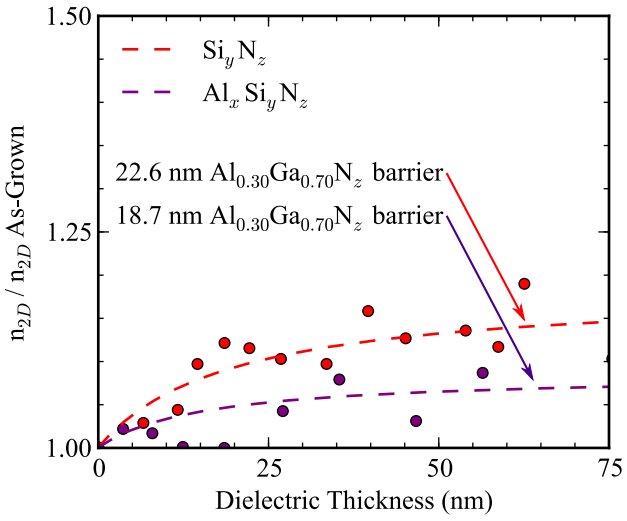

Figure 3.3: Results of the measurement of n_{2D} by C-V by thinning the deposited dielectric down from 75 nm till it was completely removed, in steps, for both Si_yN_z and $Al_xSi_yN_z$ passivations. The dashed lines represent least-squares fits to Equation 3.13, using the interface charge σ_T as the fitting parameter.

the negative polarization charge at the AlGaN surface. The smaller provision of fixed positive charge at the insulator/AlGaN interface was the reason that passivation with $Al_xSi_yN_z$ did not result in the same degree of n_{2D} enhancement that the Si_yN_z passivation indicated in Figure 3.3.

3.6 XRD Measurements

To rule out the possibility that the increased negative charge at $Al_xSi_yN_z$/AlGaN interface as compared with the Si_yN_z/AlGaN interface was a result of strain imparted to the barrier layer by the passivation, high-resolution x-ray diffraction scans were performed alongside the C-V scans in between dielectric thinning steps.

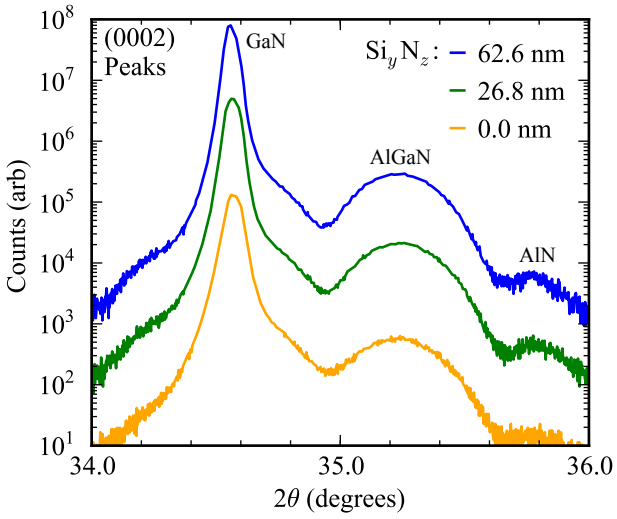

Figure 3.4: XRD scan of the (0002) GaN, AlGaN, and AlN peaks for the Si_yN_z passivated AlGaN/GaN/Al_2O_3 sample for three different thicknesses of dielectric- 62.6 nm, 26.8 nm, and 0 nm (unpassivated).

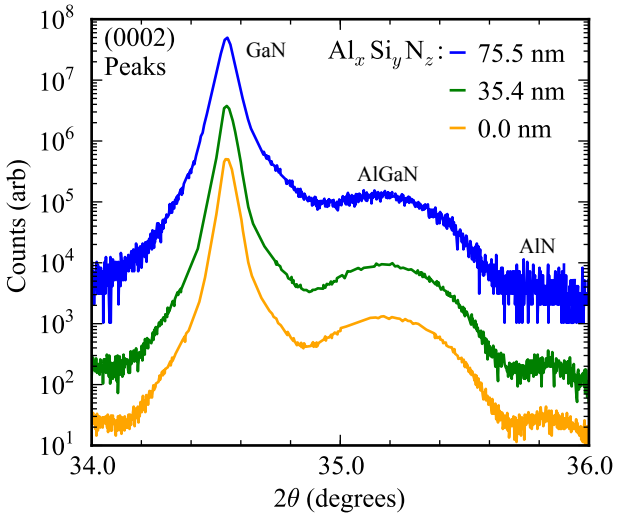

Figure 3.5: XRD scan of the (0002) GaN, AlGaN, and AlN peaks for the $Al_xSi_yN_z$ passivated AlGaN/GaN/Al_2O_3 sample for three different thicknesses of dielectric- 73.5 nm, 35.4 nm, and 0 nm (unpassivated).

If strain were being imparted to the barrier by the passivation, wet etching the passivation should slowly release strain as the dielectric thins. This release of strain should result in a noticeable shift in the AlGaN peak relative to the GaN peak, the latter of which should not move due to its thickness and being fully relaxed. Any shifts in the AlGaN peak can be related to in-plane stress by widely published elastic contants for this material system [2]. Plotted in Figures 3.4 and 3.5 are XRD scans of Si_yN_z and $Al_xSi_yN_z$ passivated AlGaN/GaN heterostructures, respectively, for three different passivation thicknesses. Clearly visible are the GaN, AlGaN, and AlN (0002) peaks in their expected positions [2]. Figures 3.6 and 3.7 show the (scaled) AlGaN (0002) peak in detail for Si_yN_z and $Al_xSi_yN_z$ passivated samples, respectively, for three different passivation thicknesses.

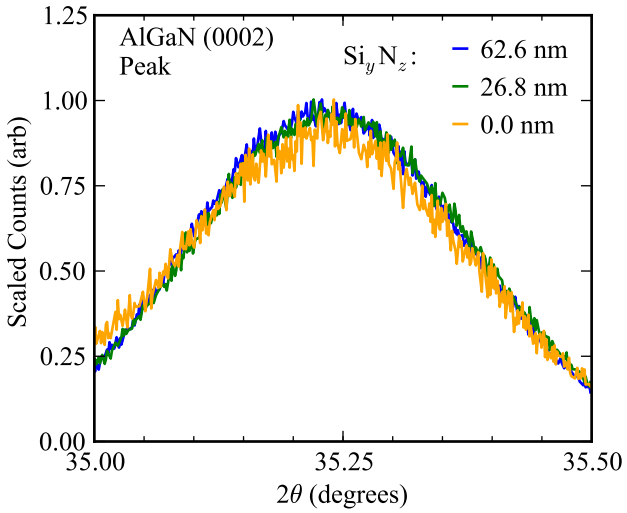

Figure 3.6: XRD scan of the (0002) AlGaN peak for the Si_yN_z passivated AlGaN/GaN/Al_2O_3 sample for three different thicknesses of dielectric- 62.6 nm, 26.8 nm, and 0 nm (unpassivated). Peaks have been normalized in intensity to the unpassivated case.

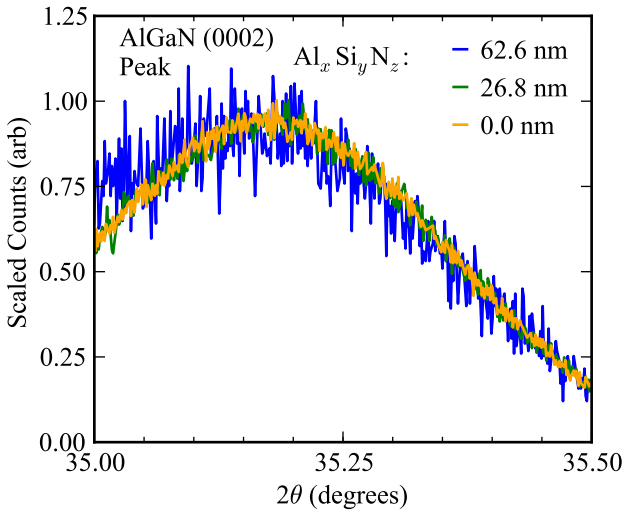

Figure 3.7: XRD scan of the (0002) AlGaN peak for the $Al_xSi_yN_z$ passivated AlGaN/GaN/Al_2O_3 sample for three different thicknesses of dielectric- 62.6 nm, 26.8 nm, and 0 nm (unpassivated). Peaks have been normalized in intensity to the unpassivated case.

No AlGaN peak shift was noted for either passivation at any thickness investigated. From these data we conclude that the apparent lack of fixed positive sheet charge at the $Al_xSi_yN_z$/AlGaN interface was not a result of barrier strain effects but a real fixed charge arising from the deposition/film chemistry itself. The consequences of the fixed negative charge are explored in more detail in Chapter 5, where the Si_yN_z and $Al_xSi_yN_z$ films are compared as AlGaN HEMT device passivations.

CHAPTER 4

FABRICATION OF LPCVD PASSIVATED ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

4.1 Introduction

In order to compare the performance characteristics of Si_yN_z and $Al_xSi_yN_z$ AlGaN/GaN HEMTs, a fabrication process for these devices keeping all parameters but the dielectric deposition itself identical was needed. As discussed in Chapter 1, the use of LPCVD dielectrics for the device passivation complicates the device fabrication as all metal contacts must be made to the surface of the device after the deposition of the passivation is complete due to the high temperature nature of the dielectric deposition. This involves both the etching of the dielectric to create regions for ohmic and gate contacts as well as lifting-off the metal contacts into these openings. This chapter illustrates the development of a fabrication process to effectively fabricate both Si_yN_z and $Al_xSi_yN_z$ passivated HEMTs, striving to keep all processing identical between the two types of passivated devices.

4.2 General Device Description

The target HEMT structure is depicted in cross-section in Figure 4.1. Typical starting epitaxial material consisted of a thick ~1 μm GaN buffer on a SiC substrate with a 25 nm thick $Al_{0.25}Ga_{0.75}N$ barrier without a GaN cap. The devices are of the field-plate type with 50 nm extensions (L_{OV}) toward the source and

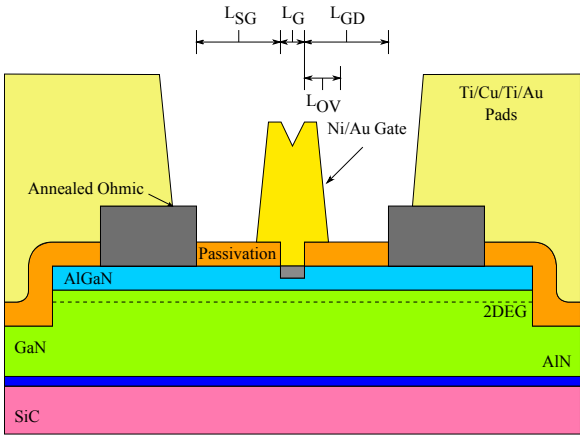

Figure 4.1: Cross-sectional schematic of target HEMT device. Mesa isolation and pad-metal is defined by photolithography and all other critical features are defined by electron beam lithography.

drain. Typical source-gate spacings (L_{SG}), gate lengths (L_G), and gate-drain spacings (L_{GD}) ranged from 0.25-0.75 μm, 50-250 nm, and 0.5-1.0 μm, respectively. All processing was performed at the Cornell Nanoscale Facility (CNF) in Ithaca, NY. Detailed processing parameters can be found in Appendix A of this document.

4.3 Alignment Marks and Active Mesa Isolation

Due to the multilevel nature of this process, alignment marks are necessary to register each lithographic layer used in processing. The two lithography tools utilized in this process are the GCA Autostep200 i-line stepper and the JEOL JBX-9300FS 100 kV electron beam lithography system (will be referred to as the "e-beam" system from here on). Both the stepper and e-beam system can recognize either etched-pit or metal alignment marks. However, as the desired first level of process is the isolation mesa level, and given both tools can register an

etched feature as an alignment mark, both the isolation mesas and alignment marks are written into the same level utilizing the stepper and roughly aligned to the corners of the sample. The mask for this process was written on a DWL 2000 laserwriter from Heidelberg Instruments Ltd.

4.3.1 i-line Photolithography Definition of Isolation Mesas and Alignment Marks

The i-line photoresist SPR955-0.9i was chosen to define both the isolation mesas and alignment marks. The sample is first placed on the resist spinner, cleaned in solvents, and spun dry. SPR955-0.9i is then applied to the surface and spin-cast at 3500 rpm with 1000 rpm/sec acceleration for 60 seconds. The resist is soft-baked at 90°C for 90 seconds, whereupon the sample is then loaded into the stepper for printing. The typical exposure times that ensured good clearing and accurate dimensions for this resist in the Autostep200 at the CNF ranged from 0.125-0.150 seconds at a defocus value of -600 nm. After exposure the resist is post-exposure baked at 115°C for 90 seconds and developed in MIF300 for 60 seconds. The patterns were then descumed in a low-power low-temperature O_2 radical process in the YES asher process #3 detailed in Appendix A. Figure 4.2 depicts the cross-section of the device at this process step.

4.3.2 ICP-RIE Etching the AlGaN Barrier

After descum, the samples were loaded into an inductively coupled plasma reactive ion etcher (ICP-RIE) and mesas and alignment marks were etched to a

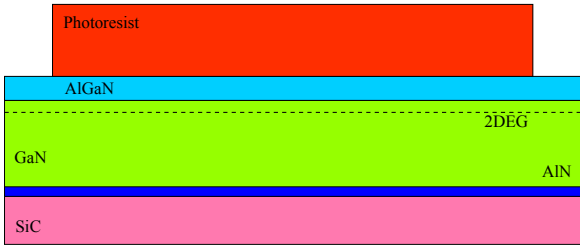

Figure 4.2: i-line photolithography to define the active device areas was well as alignment marks. 1 μm of SPR955-0.9i resist is patterned in a GCA Autostep200 stepper.

depth of 100 nm +/- 3 nm by exposure to $Cl_2/BCl_3/Ar$ (20/8/5 sccm) plasma at 25 mTorr with 50 W RIE and 400 W ICP power. The plasma self-bias was ~100 V for this process and 45 seconds of etching yielded a depth of 100 nm into the epitaxial structure (Figure 4.3 (A)). This depth was more than enough to isolate the mesas and provide high-contrast alignment marks for both the e-beam system and stepper. The residual resist is then stripped in n-methyl-pyrrolidone (NMP), rinsed in water and then exposed to a high-temperature high-power O_2 radical clean in the Aura1000 process #03F (detailed in Appendix A) to remove any plasma-hardened resist that the solvent could not remove (Figure 4.3 (B)). SEM images of the e-beam alignment marks, and the isolation mesas are shown in Figure 4.4 (A) and (B), respectively.

4.4 Device Passivation

The etched and plasma cleaned mesas were then acid-cleaned in a 1:1 solution of HCl:H_2O for 10 minutes and loaded into the LPCVD system. The typical thickness of the Si_yN_z or $Al_xSi_yN_z$ passivations used in this process was 30 nm and the details of its deposition are detailed in Chapter 2. The cross-section of

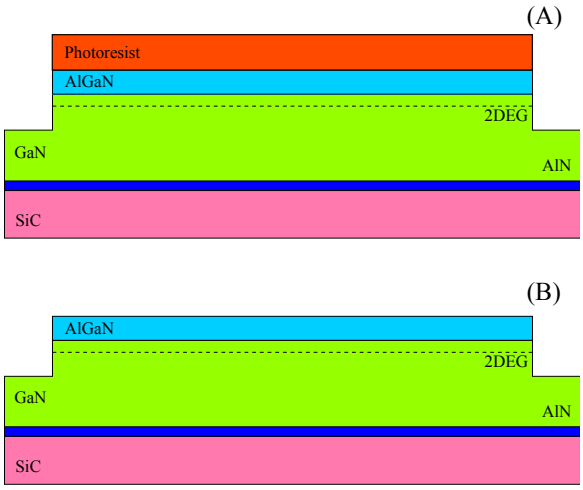

Figure 4.3: ICP-RIE etch performed in $Cl_2/BCl_3/Ar$ chemistry with resist mask. Mesas are etched to a depth of 100 nm. Resist is stripped in a combination of NMP and hot O_2 radical exposure.

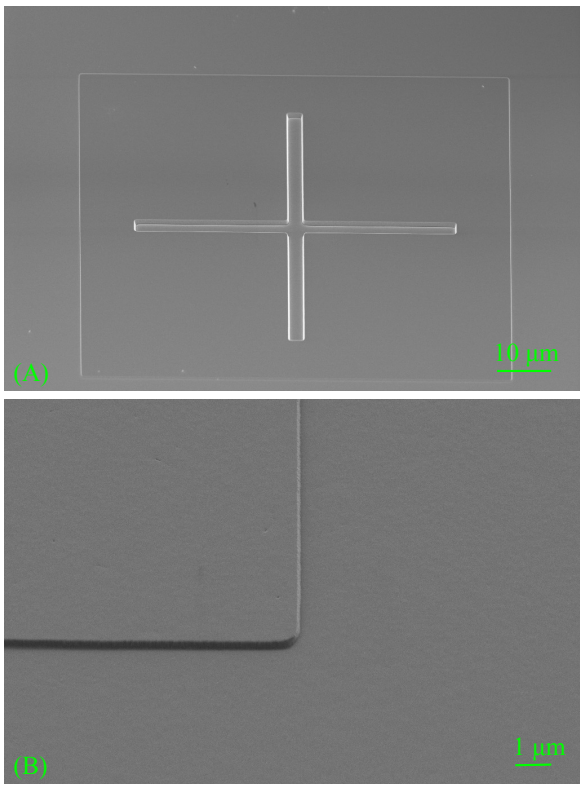

Figure 4.4: Oblique SEM images of etched electron-beam alignment marks (A), and device isolation mesas (B). Electron beam lithography tool tolerated alignment marks as shallow as 50 nm; Hence the marks were written in the same level as the isolation mesas.

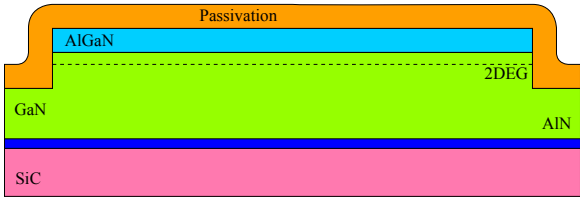

Figure 4.5: As described in Chapter 3, Si_yN_z or $Al_xSi_yN_z$ passivations were applied to the etched mesa via LPCVD. Typical thickness for both types of passivation was 30 nm.

the device at this point in processing is shown in Figure 4.5.

4.5 Gate Window Etch

As the device passivation is already present before the application of the Schottky gate in a field-plate type device, a window must be cut in the dielectric to allow the gate metal to make contact to the barrier. The dimension of this window determines the gate-length of the device - not the actual gate-metal dimension as in a T-gate device. To realize devices with large f_T and f_{MAX} with good large-signal performance in the L to Ka microwave bands, the window dimension along the channel must be kept smaller than a micron. Higher frequency performance is realized by scaling the length of the gate-etch window smaller and smaller, and the devices in this study were investigated with gate-lengths ranging from 50-250 nm. Dimensions on this order require the use of a thin (~100 nm) e-beam resist to resolve the printed features. This limitation complicates device fabrication as the etch rate of the resist relative to the passivation will determine how thick the passivation can be deposited. The limitation further complicates processes where a gate-recess etch on the barrier is desired- as this would also require a thicker resist. In studying the etch rate of Si_yN_z and

$Al_xSi_yN_z$ passivations in various etch chemistries, it was found that the $Al_xSi_yN_z$ passivation was universally more difficult to etch than the Si_yN_z passivation. Hence to study devices passivated with equal thicknesses of the two types of passivation the etching must be masked by something other than resist. For this application a hardmask consisting of a thick (150 nm) PECVD amorphous carbon layer capped with a thin (5 nm) evaporated SiO_2 layer was utilized as it provided good etch resistance to an etch chemistry that had appreciable etch rates for both the Si_yN_z and $Al_xSi_yN_z$ passivations. The amorphous carbon had the convenient advantage that it could be dry-etch patterned in an O_2 RIE process that was innocuous to the SiO_2 layer on top of it and the thin SiO_2 layer was easily patterned with resists with thicknesses on the order of 100 nm in a standard CHF_3/O_2 chemistry. Hence a thick hardmask could be created with the desired dimension by first depositing PECVD amorphous carbon, capping it with evaporated SiO_2, patterning a thin e-beam resist on top of the SiO_2, etching the SiO_2 in a CHF_3/O_2 process and then etching the amorphous carbon in an O_2 RIE. This so-called "trilevel" type patterning finds common use in the fabrication of x-ray lithography zone-plates, albeit with different hardmasking layers, but the general theory applies [132].

4.5.1 Amorphous Carbon/Evaporated SiO_2 Hardmask Deposition

The amorphous carbon is deposited in an IPE-2000 parallel-plate PECVD system from the Ion and Plasma Equipment company. Deposition occurs at 150°C at 450 mTorr, 50 W RIE, and 54 sccm CH_4. A 30 minute deposition yields 160

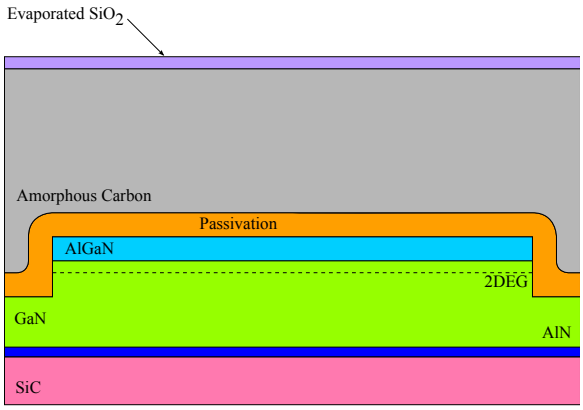

Figure 4.6: Amorphous carbon was deposited via PECVD to a thickness of 150 nm. 5 nm of SiO_2 were thereafter deposited via electron-beam evaporation.

nm of amorphous carbon. The samples are then loaded into and electron-beam evaporator system with a base pressure of 3.5 x 10^{-7} Torr and high purity SiO_2 is evaporated from pellets in a graphite crucible onto the samples which are clipped to a copper block at a rate of ~1 Å/sec. The device cross-section at this point is depicted in Figure 4.6.

4.5.2 Electron-Beam Lithography of the Gate-Window Area

ZEP520A was chosen for the lithography of the gate window regions due to both its high etch resistance and resolution. It was diluted by 1:3 (ZEP520A:Anisol solvent) from the viscosity the manufacturer provided. At the diluted viscosity, it was applied to the samples and spin-cast at 3000 rpm with an acceleration of 1000 rpm/sec for 60 seconds. It was then baked at 170°C for 5 minutes, yielding a film thickness of 100 nm. As the sample substrate as semi-insulating SiC, the sample overall was a good insulator. This can cause problems in e-beam lithography as the writing beam can charge a non-conducting sam-

ple which will cause beam deflections resulting in poor alignment and pattern resolution. To mitigate this problem, a common method employed is the evaporation of a conducting layer on top of the resist that can be later wet etched away. 150 Å of electron beam evaporated Al was chosen for this task, as it is easily removed in common photoresist developers such as MF321, which are innocuous to to the underlying ZEP520A layer. Pattern writing is performed in the e-beam system at 2 nA writing current with a dose of 750 $\mu C/cm^2$. After the exposure is complete the samples are immersed in MF321 for 90 seconds to remove the Al layer and then developed in cold (~5°C) n-amyl-acetate to develop the ZEP520A. A test sample was ran with gate window etch patterns of varying length to determine by SEM inspection the relation between designed dimension and real dimension printed in the resist. The results of this study are plotted in Figure 4.7. It is noted that the designed dimensions are smaller than the measured dimensions, hence the designed dimensions must be biased appropriately smaller to realize the indended dimensions in the developed resist.

4.5.3 RIE Etch of the Hardmask

Using the patterned ZEP520A as a mask, the SiO_2 layer was etched in a Oxford 80 parallel plate RIE system from Oxford instruments. The etch consisted of CHF_3/O_2 (50/5 sccm) chemistry at 55 mTorr, and 150 W RIE power for 30 seconds. Due to the thinness of the SiO_2 layer, an accurate etch rate could not be determined, but this etch time was found to be more than enough to pattern the SiO_2 layer and leave behind at least 30 nm of ZEP520A (Figure 4.8 (A)). The system was then pumped down to a base pressure of 1 x 10^{-5} Torr and the chemistry switched to O_2 (50 sccm) at 60 mTorr, with 150 W RIE power. This

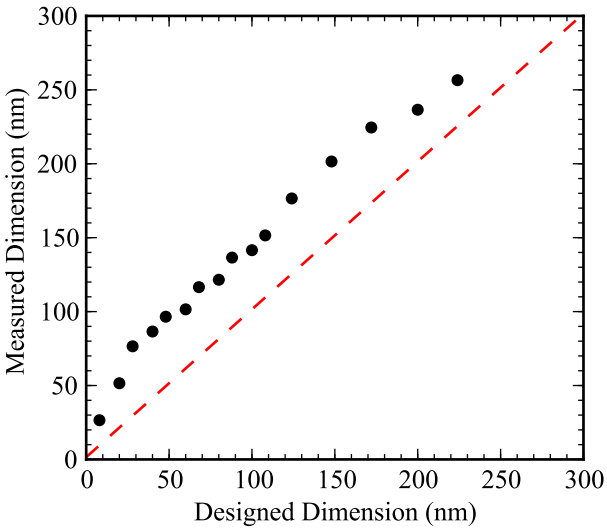

Figure 4.7: Plot showing the relation of SEM measured dimensions of gate-etch patterns vs. the designed dimension of such patterns. The dashed line indicates a 1:1 relation. From the plot it is evident that the designed size must be biased below the desired printed dimension.

etch was performed for 5 minutes - a large overetch to ensure clearing to the bottom of the amorphous carbon layer (Figure 4.8 (B)). The large overetch was made possible by the fact that both the SiO_2 covering the carbon and the passivation layer underneath the carbon are not attacked by O_2 plasma chemistries. A cross-sectional SEM image of the pattern carbon is shown in Figure 4.9, the hardmask in this image was deposited on Si for easy cleaving.

4.5.4 ICP-RIE of Dielectric/AlGaN Barrier

As previously stated, the $Al_xSi_yN_z$ films were found to etch considerably slower (~5-10x) than Si_yN_z films in common fluorine based Si_yN_z plasma etch chemistries such as CF_4, CHF_3/O_2, and SF_6. Even with the hardmask, the longer

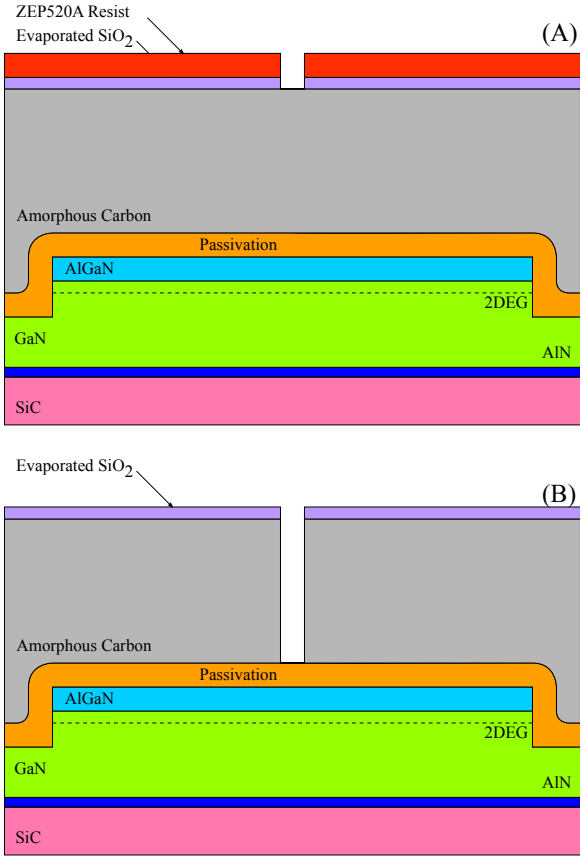

Figure 4.8: Gate-etch patterns were written in 100 nm of ZEP520A resist (A), and a CHF_3/O_2 RIE etch was used to transfer the pattern to the evaporated SiO_2. The SiO_2 mask was used to etch the amorphous carbon in an O_2 RIE etch.

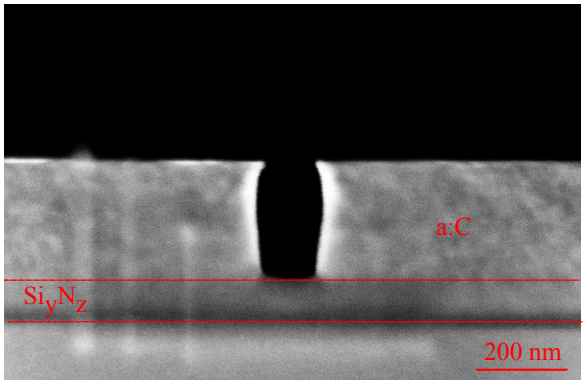

Figure 4.9: Cross-section SEM image of the completed C/SiO_2 hardmask definition. Openings in the carbon could be patterned down to ~30 nm.

etch time of the $Al_xSi_yN_z$ made using a fluorine based chemistry impractical as the hardmask would be consumed by the etch time required for the passivation. One explanation for the slower etch rate on $Al_xSi_yN_z$ could be the formation of aluminum fluorides by the reaction of the plasma chemistry with the Al in the film. Aluminum fluorides are not volatile at room temperature [133], and will thus slow the etch rate of the film if formed. This mechanism has been proposed by groups studying the effect of adding SF_6 to chlorine containing plasma chemistries employed for the etching of AlGaN [134,135]. It was noted in these studies that the etch rate of the AlGaN was significantly slowed by the addition of small amounts of SF_6 to the plasma chemistry with all other conditions being kept equal. However, as chlorine based plasma chemistries efficiently etch Al by the formation of aluminum chlorides which are volatile at room temperature, the addition of BCl_3 to a SF_6/Ar plasma chemistry which was found to efficiently etch Si_yN_z was investigated for the etching of both the $Al_xSi_yN_z$ and Si_yN_z passivations.

SF_6/BCl_3/Ar ICP-RIE Etch

An ICP-RIE plasma etch tool was employed for this etch, as the plasma self bias voltage can be tuned independently of the etch rate by employing a larger ICP power to create a denser plasma. The etch was performed in a PT-770 tool manufactured by the PlasmaTherm corporation. By varying several processing parameters such as RIE and ICP power, pressure, and gas flow ratios, an etch consisting of SF_6/BCl_3/Ar (10/10/5 sccm), at 10 mTorr, with 50 W RIE power, and 500 W ICP power was settled upon. It had a plasma self bias voltage of ~100 V and was found to etch Si_yN_z at 13.5 nm/min and $Al_xSi_yN_z$ at 9.4 nm/min, and

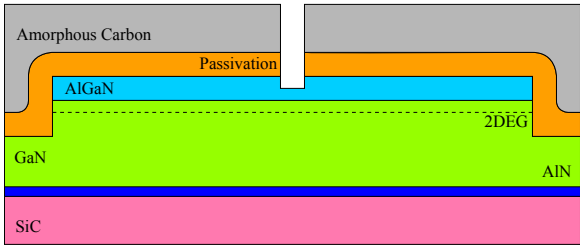

Figure 4.10: The gate-window dielectric etch and barrier-recess were performed in one step using a $SF_6/BCl_3/Ar$ ICP-RIE etch.

the amorphous carbon mask at 25 nm/min. Due to the presence of chlorine in the plasma chemistry a small, but controllable etch rate on the AlGaN barrier was observed. As can be seen in Figure 4.11 (A), C-V measurements of barrier thickness before and after exposure to this etch for varying times indicate a measurable and controllable etch rate on the barrier. Figure 4.11 (B) shows C-V measurements of the barrier post etch and post 700°C N_2 RTA annealing. We see that annealing the sample post etch further reduces its thickness, likely due to the evaporation of a volatile (at the anneal temperature, but not room temperature) etch product which the C-V measurement interprets as actual barrier material until it is removed by the anneal. This measurement gives validity to the assumption that aluminum fluorides are being formed by the reaction of the fluorine in the plasma and the aluminum in the passivation and barrier. Appropriate etch times were chosen to give a 10% overetch on the dielectric to pattern the gate window openings. The device cross-section at this point of process is shown in Figure 4.10.

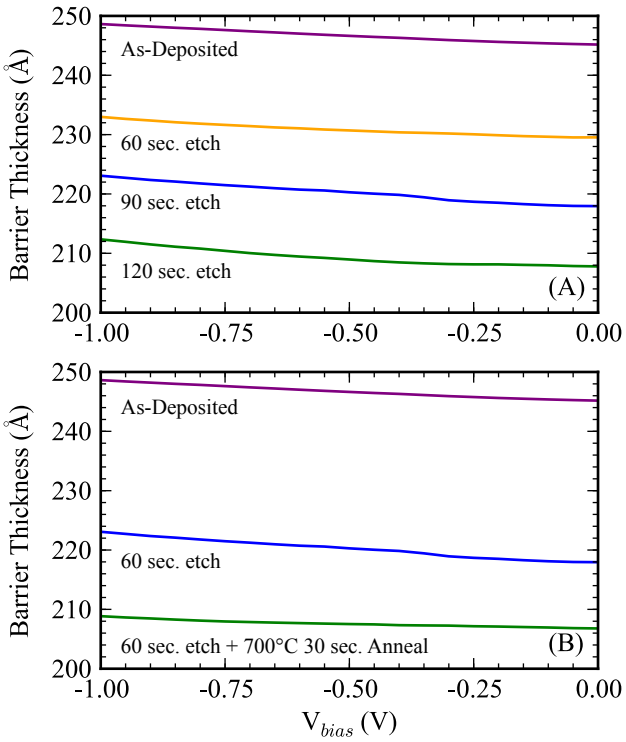

Figure 4.11: Plot showing the barrier thickness measured by C-V on an $Al_{0.25}Ga_{0.75}N$/GaN HEMT structure with a 25 nm barrier exposed to varying times in an ICP-RIE $SF_6/BCl_3/Ar$ plasma (A), and the effect of post-etch anneal (B). The barrier is shown to further thin with post etch annealing, indicating the removal of volatile products formed during etching.

4.5.5 Hardmask Strip and Etch Damage Anneal

After etching the hardmask was easily stripped in the same high-temperature high-power O_2 radical etch used to clear the photoresist from the patterned mesas and alignment marks. The sample was then annealed at 700°C in a N_2 purged RTA for 60 seconds to anneal RIE etch damage and to remove the etch product formed by the $SF_6/BCl_3/Ar$ plasma etch. The device cross-section at this point of process is shown in Figure 4.12.

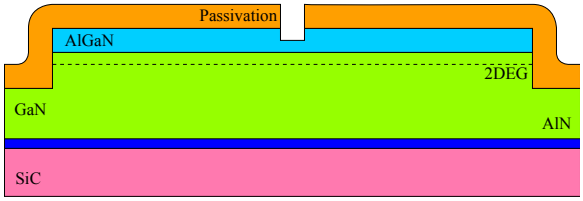

Figure 4.12: The remaining carbon hardmask was stripped using a hot O_2 radical exposure. CV measurements indicated that the 2DEG of unpassivated AlGaN/GaN heterostructures was unaffected by this process.

4.6 Source and Drain Ohmic Contacts

Windows for source and drain metallization must also be opened in the dielectric. Due to the larger size of these dimensions, a much thicker e-beam resist was employed and eliminated the need for a hardmask. A bilayer of undiluted ZEP520A (500 nm) on top of LOR3A (300 nm) was used to pattern the areas for source and drain window etches as well as the metal lift-off mask. The ZEP520A was developed in n-amyl-acetate which does not affect the underlying LOR3A. The LOR3A was developed in MF321 (TMAH based) which does not affect the ZEP520A on top. The LOR3A develops isotropically, leaving an undercut profile which is necessary for metal lift-off. The mask served to both define the etch windows as well as the lift-off of the metal. Since the same mask was used for both of these operations, the deposited ohmic metal is self-aligned with the etch windown - allowing for tighter source-gate and gate-drain spacings than if two lithography steps were used.

4.6.1 Bilayer Resist Definition

An adhesion layer for the LOR3A was found to be beneficial as it often had trouble adhering to the passivation underneath. The AR3 antireflection coating from Brewer Science was employed for this task. It was spin-cast at 5000 rpm with an acceleration of 1000 rpm/sec for 60 seconds and baked at 225°C for 5 minutes, resulting in a 65 nm film. The LOR3A was then spin-cast on top of the AR3 at 3500 rpm with an acceleration of 1000 rpm/sec for 60 seconds and baked at 170°C for 5 minutes. ZEP520A was then subsequently spin cast on top of the LOR3A at 2000 rpm with an acceleration of 1000 rpm/sec for 60 seconds and baked at 170°C for 5 minutes. As this layer was also defined using the e-beam system a 150 Å thick Al layer was again evaporated onto the resist stack to mitigate charging effects. The patterns were written in the e-beam system at a writing current of 2 nA with a dose of 300 μC/cm^2. The Al was stripped by MF321 immersion for 90 seconds and the ZEP520A was developed in cold (~5°C) n-amyl-acetate. Again, designed size biasing was used to realize the intended dimensions in the developed resist. Table 4.1 lists the designed dimensions vs. the SEM measured dimensions for the exposure and development conditions listed above. To undercut the ZEP520A, the LOR3A was developed in MF321 for 75 seconds, yielding ~200 nm of undercut underneath the ZEP520A. Figure 4.14 (A) shows a cross-section of the resist stack on Si after the development of the ZEP520A and Figure 4.14 (B) shows the stack post MF321 development for 75 seconds. It is clear from these images that the two developers do not interfere with anything but the intended resist.

Table 4.1: Table indicating the relation of SEM measured dimensions of ohmic source and drain patterns vs. their designed dimension. The CAD designed dimensions must be appropriately biased to a smaller size than desired as was the case with the gate-etch dimensions.

Designed Dimension	Measured Dimension
3.850 μm	4.000 μm
3.900 μm	4.026 μm
3.950 μm	4.093 μm
4.000 μm	4.145 μm

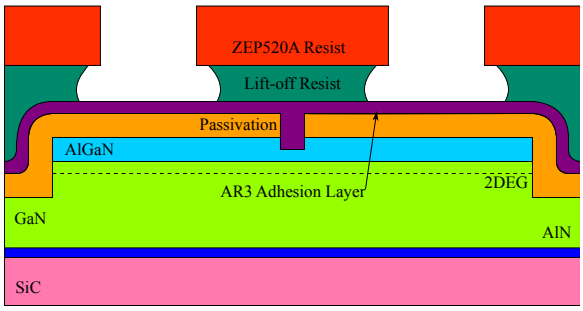

Figure 4.13: Resist bilayer used to etch the dielectric for the source/drain regions as well as lift off the ohmic metal for these contacts. A thin (65 nm) thick layer of AR3 antireflection coating was used to enhance the adhesion of the LOR (300 nm) lift-off resist as it often had adhesion issues when used in conjunction with the (500 nm) ZEP520A resist. Development of the ZEP520A was with accomplished with n-Amyl-Acetate, while the development of the LOR resist was accomplished with MF321 (TMAH based).

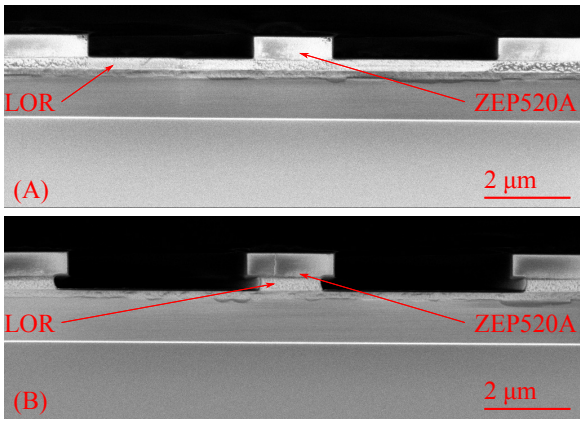

Figure 4.14: Cross sectional SEM image of developed ZEP520A resist for the source/drain regions (A), and the developed LOR resist (B). The developers for both types of resist were not found to affect the other (non-developed) resist.

4.6.2 RIE Dielectric Etch

After the development of the LOR3A, there still remains he AR3 adhesion layer. This layer removed by a 25 second O_2 RIE etch in the Oxford 80 with 50 sccm O_2 at 60 mTorr, and 150 W RIE power (Figure 4.15 (A)). The dielectric is then etched in the same etcher with a CHF_3/O_2 (50/5 sccm) chemistry at 55 mTorr and 150 W RIE (Figure 4.15 (B)). The Si_yN_z and $Al_xSi_yN_z$ had etch rates of 40 nm/min and 7 nm/min, respectively. The ZEP520A had an etch rate of ~40 nm/min in this recipe, hence there was plenty present to etch through the 30 nm of passivation present on the samples.

4.6.3 Ohmic Metal Evaporation/Lift-Off

After etching the samples were then cleaned in a 1:1 HCl:H_2O mixture for 5 minutes and loaded into an electron beam evaporation system with a base pres-

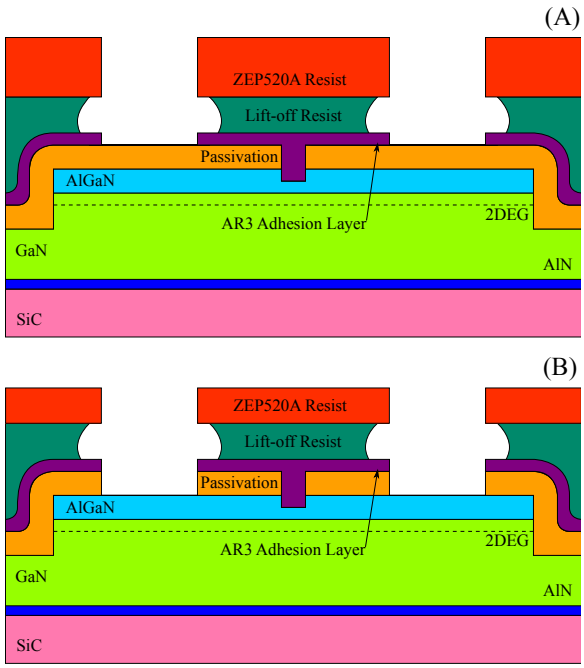

Figure 4.15: The AR3 adhesion layer is cleared in a 25 second O_2 descum RIE (A), followed by the etching of the passivation for the source/drain regions in a CHF_3/O_2 RIE (B).

sure of 3.5 x 10^{-7} Torr base pressure. For the HEMT devices described in Chapter 6 a Ta/Ti/Al/Mo/Au (125/150/900/400/500 Å) multilayer was evaporated through the ZEP/LOR lift-off mask, but the mask works equally well for other metal stacks less than 300 nm thick (the thickness of the LOR) such as the metallizations described in the study found in Chapter 6. Lift-off of the unwanted metal is accomplished by immersion in NMP and water rinsing. The AR3 coating is however not removed by the NMP, it must be ashed. A high-power low-temperature O_2 radical exposure was performed in the YES asher process #12 (see Appendix A) is used to clear the AR3 and clean up any residual organic material left behind.

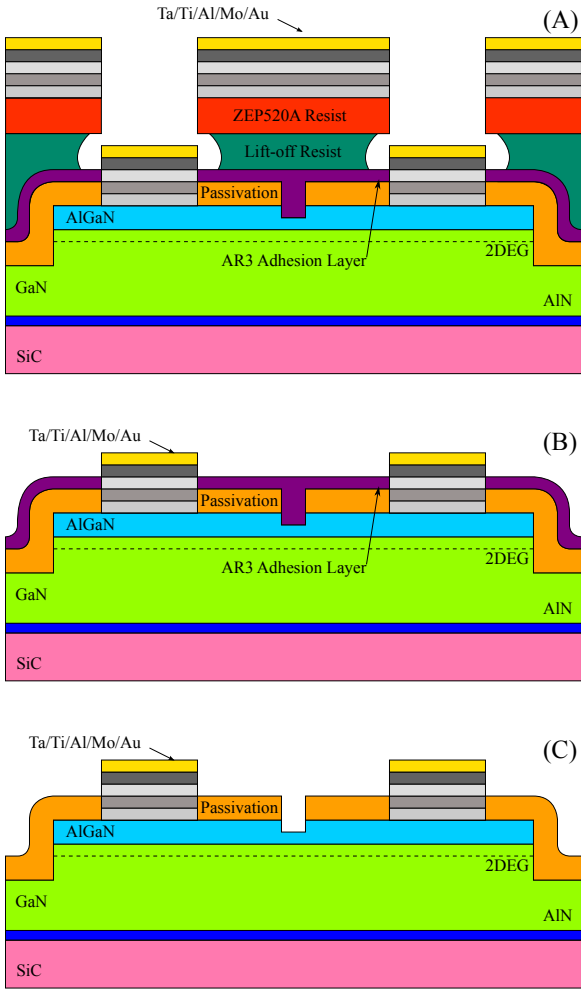

Figure 4.16: Samples are cleaned in HCl:H_2O (1:1) for 5 minutes and then loaded into an electron-beam evaporator for the deposition of the ohmic metal (A). Resist and unwanted metals were lifted off in NMP (B) and the remaining AR3 was cleared in a low-temperature O_2 radical exposure (C).

4.6.4 Ohmic Metal Anneal

The ohmic metal was annealed in an N_2 purged RTA at 700°C for 1 minute followed by an 800°C anneal for 30 seconds (Figure 4.17). This yielded a contact resistance of ~0.3 Ω-mm. Occasionally this metal stack/annealing condition caused problems with the ohmic flowing beyond the lithographically defined

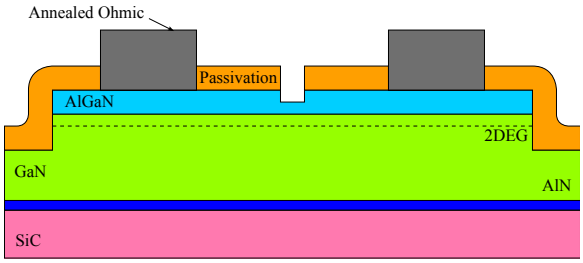

Figure 4.17: Samples were loaded on a graphite susceptor in a N_2 purged RTA annealed at the activation temperature of the ohmic metal. For the devices described in Chapter 6, the optimum temperature/exposure time was found to be 700°C/1 minute followed by 800°C/30 seconds.

dimensions. It seemed very sensitive to the ramp rate of the anneal and the passivation type and did not happen consistently. A solution to this problem was found that minimally alters the process and is presented in Chapter 6.

4.7 Gate Metal

Schottky contacts need to be made to the exposed AlGaN layer in the gate window to allow control of the channel charge between source and drain. Evaporated Ni/Au (25/300 nm) was utilized for this purpose. To define the lift-off mask for this metal e-beam lithography is used to pattern a bilayer of PMMA (495k MW - 600 nm) and PMMA (950k - 100 nm) spin cast on the sample. The PMMA 495k develops more quickly than the 950k MW resist on top of it, resulting in an undercut suitable for lift-off.

4.7.1 Bilayer Resist Definition

The PMMA 495k "A8" (set in anisol) was spin cast on the sample at 3000 rpm with an acceleration of 1000 rpm/sec for 90 seconds and baked at 170°C for 15 minutes. PMMA 950k (set in MIBK) was then spin cast on top of the 495k PMMA layer with identical spin and bake parameters. Again, a 150 Å layer of Al was employed as a charge dissipation layer. Exposure was carried out with a 2 nA writing current and a dose of 1800 $\mu C/cm^2$. After exposure the Al was stripped by immersion in MF321 for 90 seconds (which does not affect the PMMA) and the PMMA bilayer was developed with a 45 second immersion in 1:1 MIBK:IPA mixture resulting in the cross section seen in Figure 4.19. Figure 4.18 shows the relation between designed gate-metal pattern vs. SEM measured pattern. Again, smaller than intended dimensions needed to be designed to realize the intended ones.

4.7.2 Gate Metal Evaporation/Lift-Off

After the PMMA bilayer development the samples were then cleaned in a 1:1 HCl:H_2O mixture for 5 minutes and loaded into an electron beam evaporation system with a base pressure of 3.5 x 10^{-8} Torr base pressure (Figure 4.20 (A)). Ni and Au layers were evaporated to a thickness of 25 and 300 nm, respectively and the unwanted metal was lifted-off in dichloromethane (Figure 4.20 (B)).

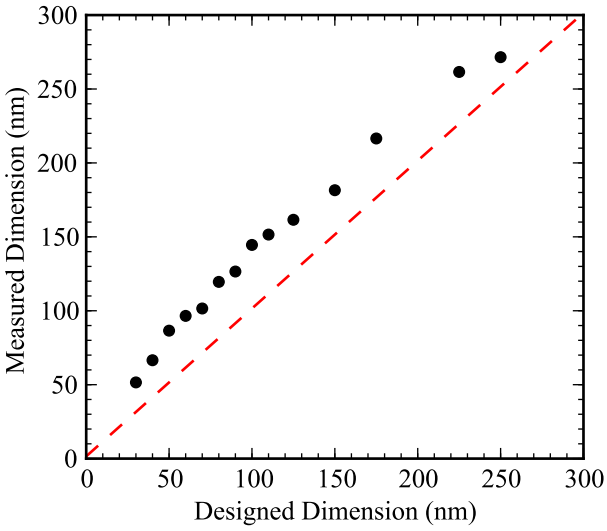

Figure 4.18: Plot showing the relation of SEM measured dimensions of gate metal patterns vs. the designed dimension of such patterns. The dashed line represents a 1:1 relation. From the plot it is evident that the designed size must be biased below the desired printed dimension.

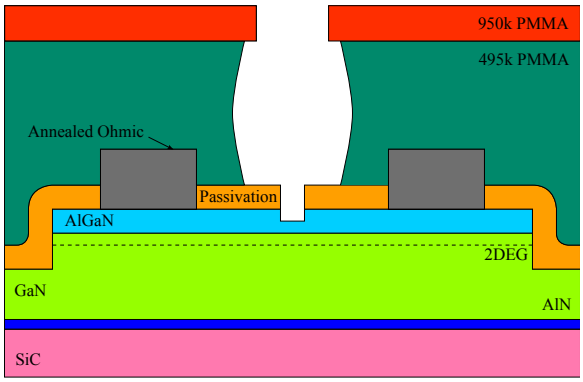

Figure 4.19: Electron-beam lithography was used to define the gate metal mask in a PMMA (495k - 600 nm)/PMMA (950k - 100 nm) bilayer. Each layer was baked at 170°C for 15 minutes. Development of the PMMA was with a 1:1 mixture of MIBK:IPA.

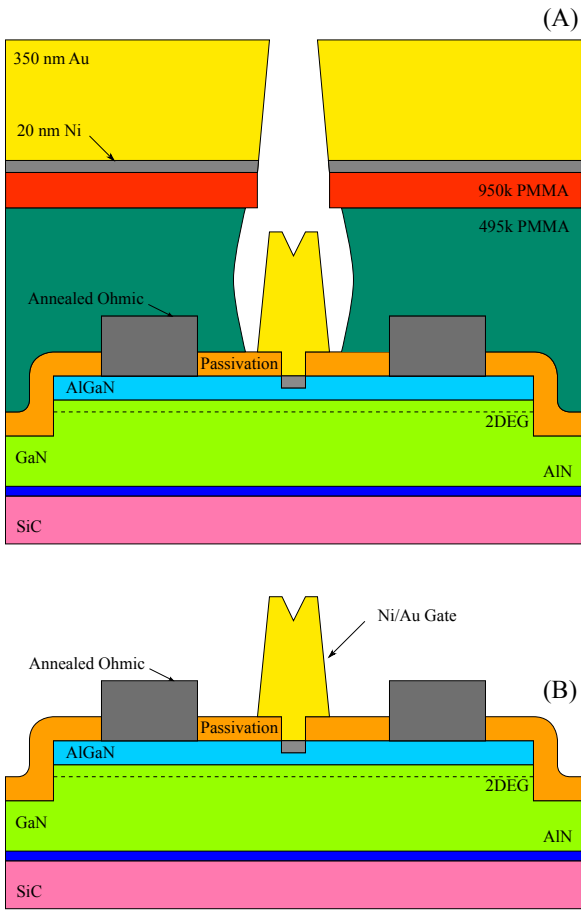

Figure 4.20: Ni/Au (25/300 nm) gate-metal is evaporated by electron beam lithography through the PMMA bilayer mask. Lift-off of the unwanted metal is accomplished in dichloromethane.

4.8 Coplanar Waveguide Pads

With the active device constructed, coplanar waveguide pads now must be lifted-off to make contact to the source, drain, and gate metallizations so that the HEMTs can be tested at microwave frequencies. i-line lithography was used to define a lift-off mask consisting of SPR955-0.9i (1 μm) on top of LOR10A (1 μm).

4.8.1 Bilayer Resist Definition

The LOR10A was spin-cast at 3500 rpm with an acceleration of 1000 rpm/sec for 60 seconds and baked at 170°C for 5 minutes. The SPR955-0.9i was spin-cast and baked in the same manner as was used to define the mesas, albeit on top of the LOR10A. The samples were loaded into the stepper and exposed with a dose between 0.125-0.150 seconds with a defocus value of -6. After post-exposure baking the SPR955-0.9i at 115°C for 90 seconds, the samples were developed for 75 seconds in MIF300. This development both defined the SPR955-0.9i as well as undercut the LOR10A, leaving an undercut profile suitable for pad metal lift-off (Figure 4.21).

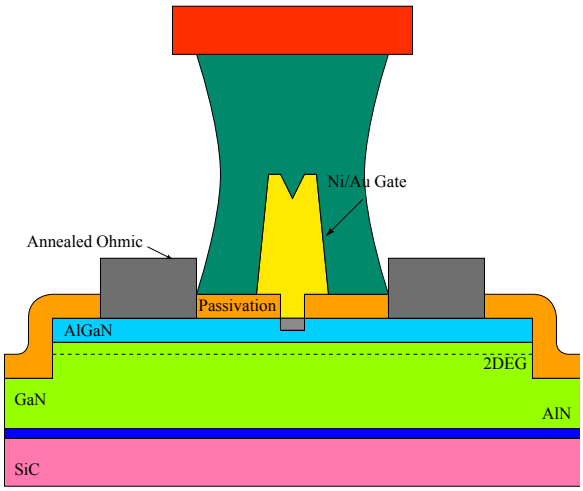

Figure 4.21: A bilayer of SPR955-0.9i on top of LOR10A is used to define the pad-metal lift-off.

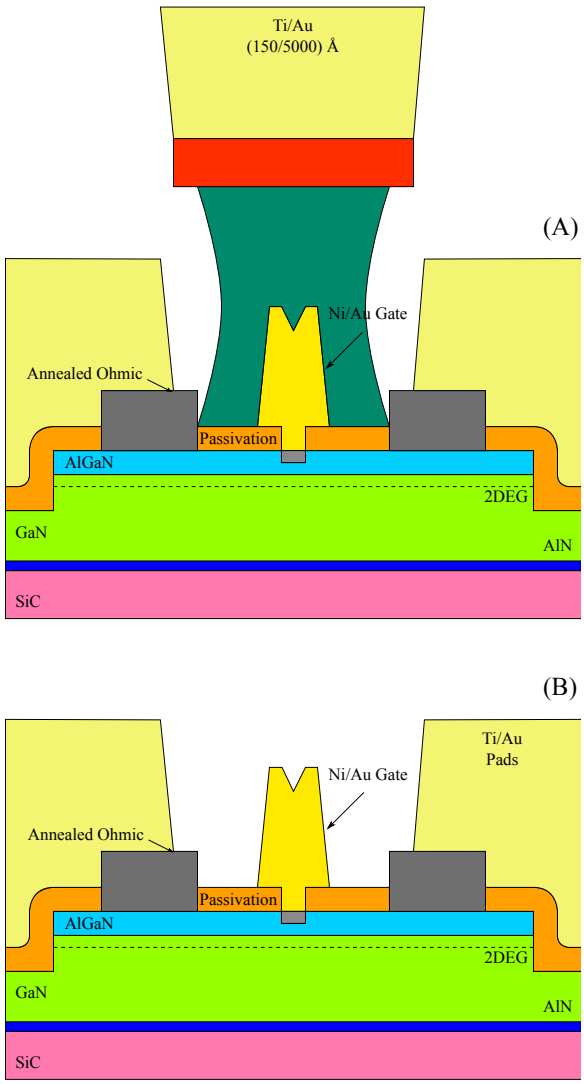

Figure 4.22: Electron beam evaporation is used to deposit the Ti/Au (15/500 nm) pad-metal (A) and NMP immersion is used to lift-off the unwanted metal (B).

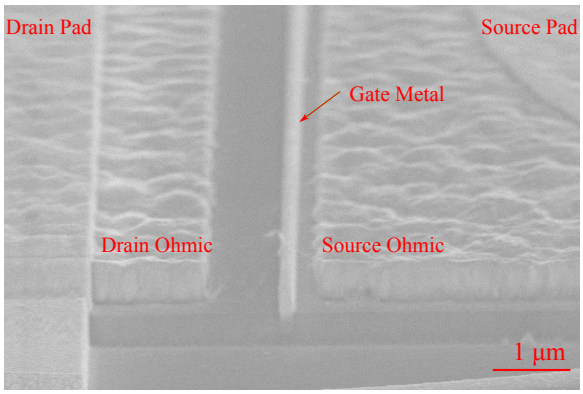

Figure 4.23: Close-up oblique SEM image of a completed HEMT active area showing all etches and metallizations described.

4.8.2 Pad Metal Evaporation/Lift-Off

After resist development a low-power low-temperature O_2 radical exposure was utilized to descum the surface of the sample where the pad-metal with eventually adhere. The samples were then loaded into the electron beam evaporator for the deposition of Ti and Au layers at 15 and 500 nm, respectively (Figure 4.22 (A)). The unwanted metal is then lifted off in NMP (Figure 4.22 (B)) to complete the device fabrication. A close-up SEM image of the active area of a completed HEMT is shown in Figure 4.23.

CHAPTER 5

CHARACTERIZATION OF SI_YN_Z AND $AL_XSI_YN_Z$ PASSIVATED HIGH ELECTRON MOBILITY TRANSISTORS

5.1 Introduction

High electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures have seen great improvements in both power-density and efficiency at increasingly higher microwave operating frequencies since their introduction. A key development enabling these improvements was the reduction of the widely reported DC-to-RF dispersion effect by surface passivation with a dielectric such as silicon nitride [8,24]. Various other passivations have since been shown to decrease this parasitic effect, however, silicon nitride deposited by CVD remains the most commonly applied [55,136,137]. Passivation of the slow surface traps with a dielectric has also been shown to increase the sheet electron density (n_{2D}) at the heterostructure interface resulting from compensation of polarization charge [43]. The increased sheet electron density leads to increased longitudinal electric fields between terminals of the device; this reduces breakdown voltage and increases DC-to-RF dispersion in the case of increased gate-drain fields, and creates a nonlinear dependence of source resistance with drain current density in the case of increased source-gate fields [57]. Reduction of n_{2D} in the gate-drain region is most commonly achieved with source or gate connected field plates, and good results have been shown with devices outputting over 30 W/mm at frequencies up to 8 GHz [55], and over 16 W/mm at 10 GHz [7]. However, the added capacitance of these extensions limit their use at higher frequencies where they present a significant parasitic load. A di-

electric passivation which ties-up the AlGaN surface traps and creates a smaller increase in n_{2D} is thus desired, as the reduction in n_{2D} would not come at the penalty of increased capacitance. In this chapter the microwave performance of HEMTs passivated with LPCVD Si_yN_z and $Al_xSi_yN_z$ is compared, the latter which we have shown in Chapter 2 to reduce the increase in n_{2D} in HEMT structures post passivation compared to an equal thickness of Si_yN_z. It is shown that the $Al_xSi_yN_z$ passivation results in devices with increased breakdown voltages, higher power densities, and (at the time of this writing) record values of PAE at both 10 and 35 GHz.

5.2 Material and Device Description

Si_yN_z and $Al_xSi_yN_z$ AlGaN/GaN HEMTs were fabricated on separate pieces of the same epitaxial material and underwent a side-by-side fabrication process to create HEMTs for the comparison of of the Si_yN_z and $Al_xSi_yN_z$ dielectrics as passivations. The details of the dielectric deposition and subsequent fabrication steps are described in chapters 2 and 4, respectively, but the pertinent details are as follows: Identical samples of epitaxial material consisting of an $Al_{0.25}Ga_{0.75}N$/GaN heterostructure grown on S.I. SiC with a barrier thickness of approximately 250 Å. Capacitance-voltage measurements of n_{2D} on the as-grown, Si_yN_z, and $Al_xSi_yN_z$ passivated samples are shown in Figure 5.1, and indicate a significantly larger value for the Si_yN_z passivated samples compared to the $Al_xSi_yN_z$ passivated samples. Transfer length method (TLM) measurements on similar samples indicated a sheet resistance of ~450 Ω/□. Active device areas were isolated by mesa etching in a $Cl_2/BCl_3/Ar$ inductively coupled plasma reactive ion etch (ICP-RIE). The Si_yN_z and $Al_xSi_yN_z$ passivations were then de-

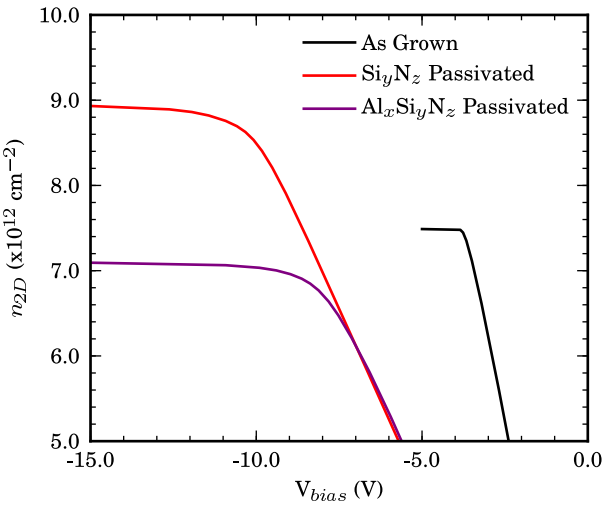

Figure 5.1: Capacitance-Voltage characterization of n_{2D} for the Si_yN_z, $Al_xSi_yN_z$, and as-grown heterostructures used in this study.

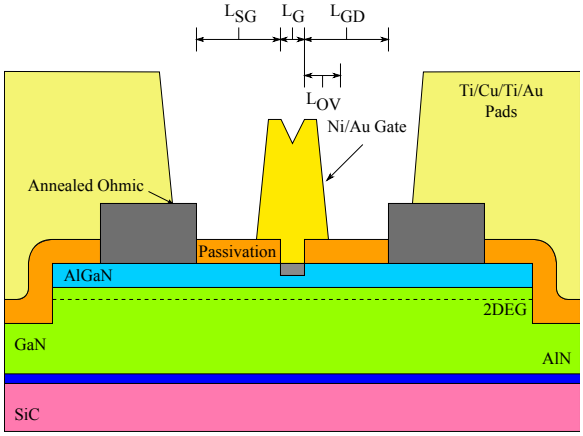

Figure 5.2: Passivated AlGaN/GaN HEMT cross-sectional schematic. Source-gate, and gate-drain spacings are indicated as L_{SG} and L_{GD}, respectively. Gate-length is indicated as L_G, and the gate metal extensions toward the source and drain are indicated as L_{OV}.

posited on separate samples at a thickness of 300 Å by LPCVD. Devices were investigated with source-gate spacings (L_{SG}), gate lengths (L_G), and gate-drain spacings (L_{GD}) of 0.25-0.65 μm, 50-250 nm, and 0.5-1.0 μm, respectively- these dimensions are depicted in Figure 5.2.

5.3 Device Measurements

The performance of Si_yN_z and $Al_xSi_yN_z$ passivated HEMTs was compared in DC, large-signal, and small-signal test environments.

5.3.1 DC and Small-Signal Characterization Setup

The device under test (DUT) was placed on a copper stage where ground-signal-ground (GSG) coplanar waveguide probes made contact to the pad connections of the HEMT. DC biasing was accomplished with an HP4142B modular source/monitor system employing a ground unit, a HP41421B medium-power SMU, and a HP41420A high-power SMU. Small-signal AC signals were provided by an HP8510C vector network analyzer equipped with a 50 GHz synthesized sweeper and S-parameter measurement unit. The output from the HP4142B was fed into bias-T's with a 1-MΩ impedance on the HP8510C and the biasing and small-signal stimuli were fed to the coplanar probes via microwave cabling. DC currents measured with the setup had to be corrected in software to account for the 1-MΩ resistance of the bias-T's.

5.3.2 DC measurements

DC measurements to determine the transfer and output characteristics of the transistors were performed on the above described coplanar waveguide probing station with biasing provided by the HP4142B unit and the HP8510C unit providing 50 Ω terminations to prevent the devices from entering a state of oscil-

lation. Device pinch-off voltage (V_{po}), transconductance (g_m), and gate leakage current (i_g) were determined by analyzing the drain current (I_D) vs. gate-voltage (V_G) at a constant drain bias of 10 V. The device output characteristics were then determined by sweeping the drain-voltage from 0-10 V at fixed gate biases ranging from -6-2 V.

Device Transfer Characteristics

The devices were measured at a drain bias (V_D) of 15 V with the source grounded and the gate voltage (V_G) swept from -5 V to 2 V. Plotted in Figures 5.3,5.4, and 5.5, respectively are comparisons of drain current (I_D), transconductance (g_m), and gate leakage current (I_g), respectively, vs. gate-bias (V_G) for identically sized Si_yN_z and $Al_xSi_yN_z$ HEMTs. From Figures 5.3, and5.4 it is evident that the $Al_xSi_yN_z$ devices received a deeper gate-recess etch than the Si_yN_z devices, as the pinch-off voltage (V_{PO}) magnitude is reduced on these devices. The pinch-off voltage, plotted in Figure 5.6, was also found to have a large dependence on L_G; with devices with longer gates having a smaller pinch-off voltage magnitude. This was likely due to the well known RIE lag effect causing the wider openings for devices with longer L_G to be etched to a greater depth than the smaller openings [138]. Devices with both $Al_xSi_yN_z$ and Si_yN_z passivations show similar maximum values of transconductance and gate leakage current, however the Si_yN_z passivated devices show a slightly reduced magnitude of gate leakage current.

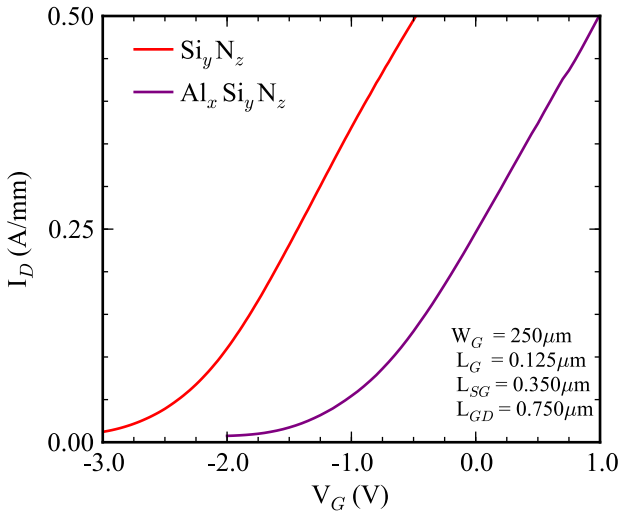

Figure 5.3: Plot of Drain current (I_D) vs. gate bias (V_G) for identically sized Si_yN_z and $Al_xSi_yN_z$ HEMTs. The deeper recess the $Al_xSi_yN_z$ devices received is evident from the smaller magnitude of pinch-off voltage on these devices.

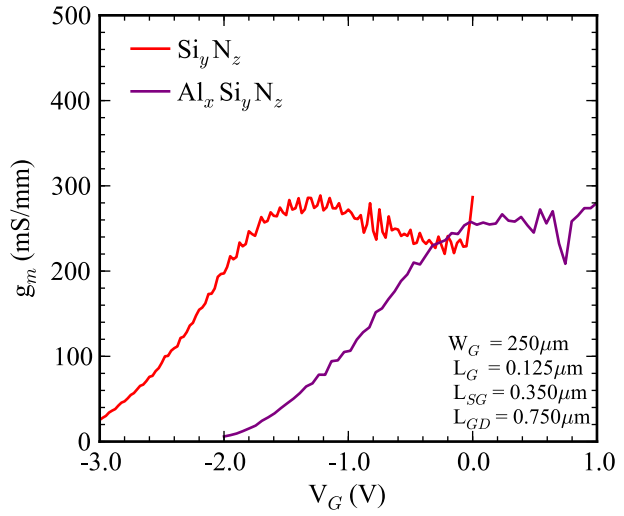

Figure 5.4: Plot of transconductance (g_m) vs gate bias (V_G) for identically sized Si_yN_z and $Al_xSi_yN_z$ HEMTs. Maximum transconductance is comparable for both types of passivation.

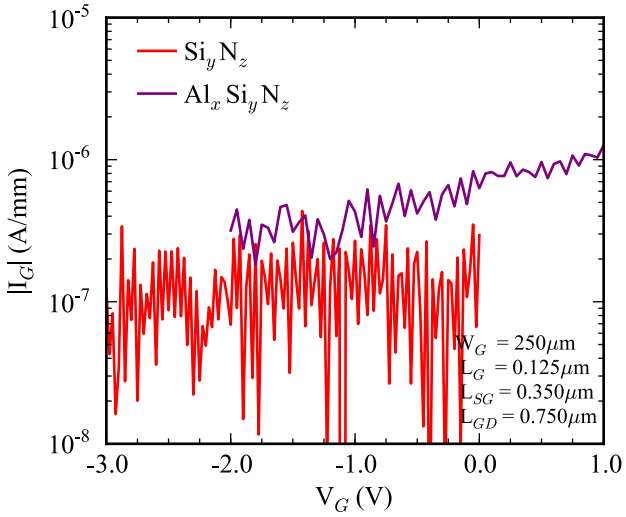

Figure 5.5: Plot of gate leakage current (I_G) vs. gate bias (V_G). Devices passivated with both Si_yN_z have a slightly reduced value of gate leakage compared to $Al_xSi_yN_z$, but the value is similar in magnitude.

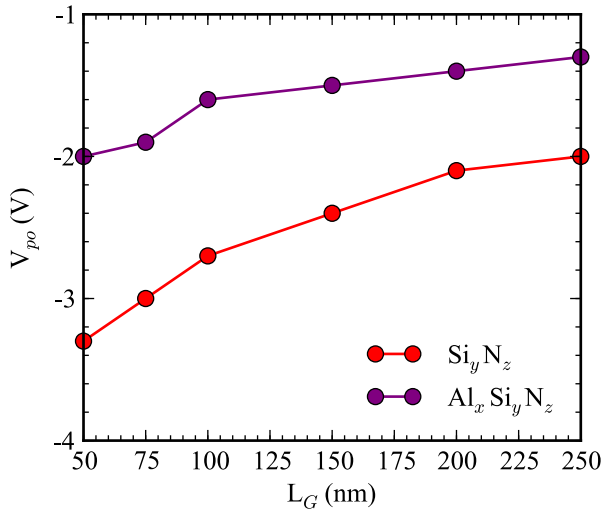

Figure 5.6: Dependence of pinch off voltage V_{PO} on gate length (L_G). The $Al_xSi_yN_z$ devices are universally observed to have a V_{PO} of smaller magnitude than the corresponding Si_yN_z devices, due to a deeper etch under the gate.

Device Output Characteristics

At gate biases ranging from -6 V to 2 V, the drain current (I_D) vs. drain voltage (V_D) for Si_yN_z and $Al_xSi_yN_z$ passivated is plotted in Figure 5.7(A) and 5.7(B), respectively. Knee voltages were around 2 V for both types of devices, indicating similar ohmic contact properties. At 10 V on the drain, both Si_yN_z and $Al_xSi_yN_z$ yielded ~0.75 A/mm drain current density. Output conductance was also similar for both the Si_yN_z and $Al_xSi_yN_z$ passivated devices and was around 10^{-6} to 10^{-7} S/mm.

5.3.3 Small-Signal Measurements

Small-signal characterization of the HEMTs was performed via S-Parameter measurements from 500 MHz to 42 GHz at appropriate biases to extract both the intrinsic and extrinsic equivalent circuit elements of the device model shown in Figure 5.8. The model is based of a previously reported model [139], with the addition of shunt conductances G_{GD} and G_{GS} to represent the leakage paths introduced by the passivation. The extraction methodology used is described in [140].

Pad and Interelectrode Capacitances

Owing to the smaller permittivity of the $Al_xSi_yN_z$ relative to the Si_yN_z, devices passivated with $Al_xSi_yN_z$ were expected to yield smaller interelectrode and pad capacitances relative to devices passivated with Si_yN_z. To the contrary, small-signal measurements revealed there was little difference in the measured gate-

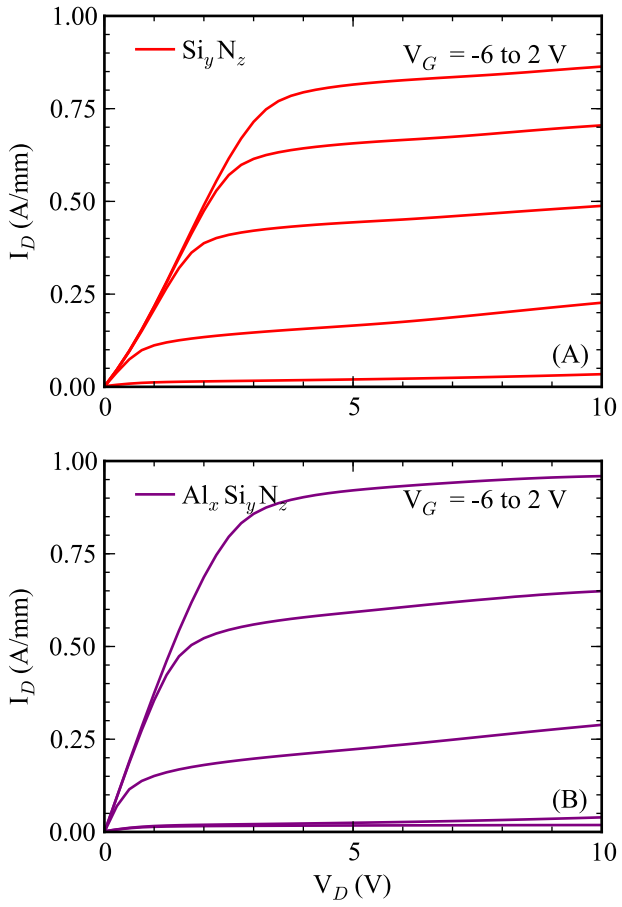

Figure 5.7: Output characteristic plot for a typical Si_yN_z and $Al_xSi_yN_z$ passivated HEMT with dimensions: W_G=100 μm, L_G=0.125 μm, L_{SG}=0.350 μm, and L_{GD}=0.750 μm.

drain, or gate-source capacitances of similarly sized $Al_xSi_yN_z$ and Si_yN_z passivated devices. The pad capacitance on the $Al_xSi_yN_z$ passivated devices was however measured to be consistently lower than that on corresponding Si_yN_z devices.

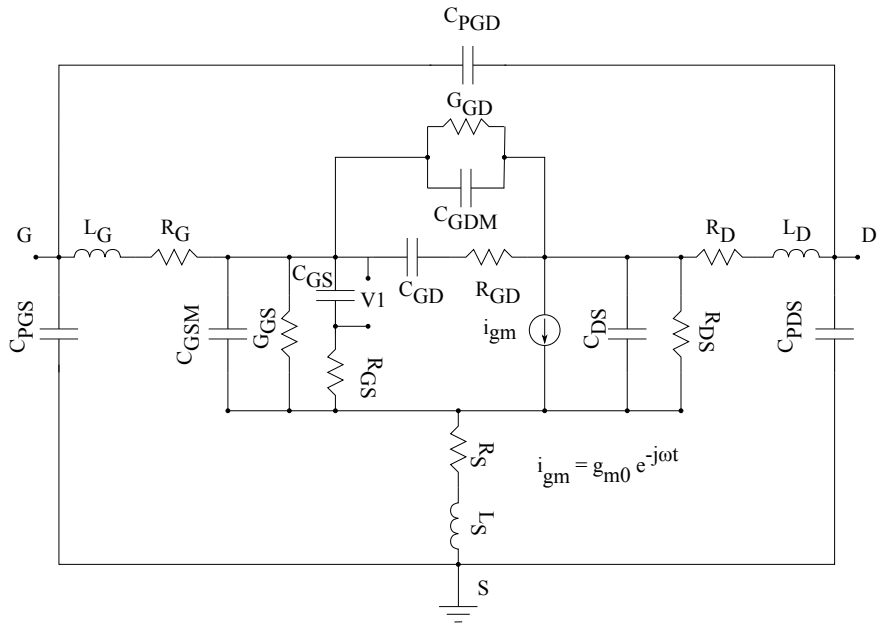

Figure 5.8: Small-signal HEMT equivalent circuit model utilized in this study.

Access Resistances

As indicated by CV measurements in Chapter 3, $Al_xSi_yN_z$ passivated HEMT structures show a reduced 2DEG density compared to Si_yN_z for equal thicknesses of passivation. Due to the smaller 2DEG density of an $Al_xSi_yN_z$ passivated structure, the access resistances (R_S and R_D) in a HEMT device are expected to be larger than a comparable Si_yN_z passivated device. However, as discussed in Chapter 1, previous studies have shown that large longitudinal electric fields existing in the ungated portions of AlGaN/GaN HEMTs, arising from the injection of high current densities, can give rise to a nonlinear increase access resistance with drain current density [57]. Reducing the 2DEG density in the ungated regions such as the source-gate region is one way to reduce these longitudinal electric fields without the use of field plates. Plotted in Figure 5.9 is the extracted source access resistance (R_S) at drain current densities up to 1

A/mm of device periphery. It is obvious that the $Al_xSi_yN_z$ passivated devices do not suffer the same nonlinear increase in R_S that the equivalent Si_yN_z passivated devices exhibit. The access resistance of the $Al_xSi_yN_z$ passivated devices was however found to be larger than that of the Si_yN_z passivated devices at lower drain current densities where the increase in resistance due to longitudinal electric fields is not expected. At ~1 A/mm drain current density, Si_yN_z passivated devices show ~4 x the source access resistance of a $Al_xSi_yN_z$ passivated HEMT of the same dimension. The drain access resistances (R_D) of both Si_yN_z and $Al_xSi_yN_z$ passivated devices are plotted in Figure 5.10, which shows that the Si_yN_z devices show a lower resistance for all drain biases tested. The lower value of drain access resistance on the Si_yN_z passivated devices is due to the smaller sheet resistance of these samples afforded by the larger value of n_{2D} this type of passivation was shown to provide. However, at the high end of drain current density, the drain access resistance of the Si_yN_z passivated devices is shown to proportionally increase to a greater degree than what is measured on the $Al_xSi_yN_z$. The larger increase in drain resistance on the Si_yN_z vs the $Al_xSi_yN_z$ passivated devices is also attributed to the increased longitudinal electric fields resulting from the larger value of n_{2D} measured on the Si_yN_z passivated structures relative to the $Al_xSi_yN_z$ structures. The larger nonlinear increase in source resistance vs drain resistance at high drain current density is due to the fact that the longitudinal electric fields created by the injection of high current densities are reduced in the gate-drain region due to the larger electrode spacing compared to the source-gate region.

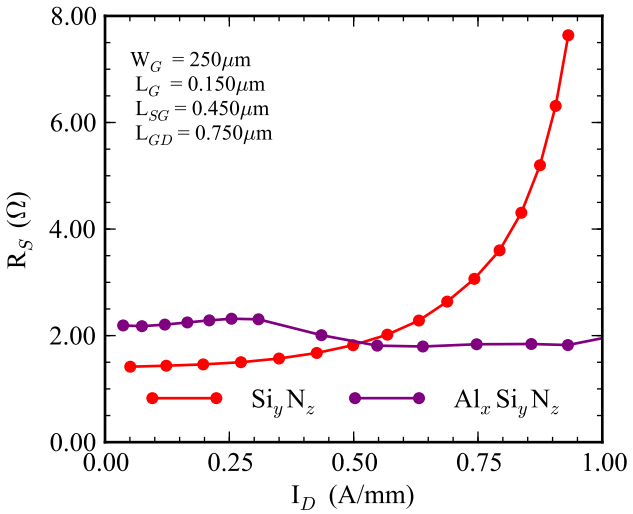

Figure 5.9: Source access resistance as a function of drain current density. Unlike the Si_yN_z passivated devices, $Al_xSi_yN_z$ passivated HEMTs show no increase in source access resistance with increased drain current density. This is attributed to the reduced longitudinal electric fields in the ungated source-gate region afforded by the smaller 2DEG density the $Al_xSi_yN_z$ passivation provides.

f_T and f_{MAX}

The extrinsic unity current gain cutoff frequency (f_T) is determined by measuring the H_{21} response of the HEMTs across the range of frequencies available to the setup (500 MHz - 42 GHz) and extrapolating the frequency at which H_{21} becomes unity on a log-log plot by assuming a 20 dB/dec slope. The extrinsic maximum frequency of oscillation (f_{MAX}) is determined in a similar manner, but by extrapolating the frequency which the magnitude of the maximum available gain (MAG) becomes unity assuming a 20 dB/dec slope on a log-log scale.

The intrinsic values of f_T and f_{MAX} are determined by first de-embedding the parasitic pad capacitances and inductances from the the H_{21} and MAG responses, as previously described [140]. A previous study [139], analyzing an

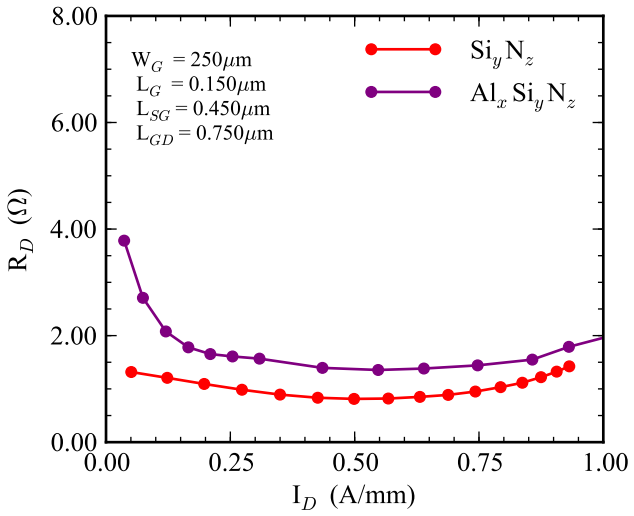

Figure 5.10: Drain access resistance as a function of drain current density. The Si_yN_z passivated devices show a reduced drain resistance due to the higher value of n_{2D} and subsequently lower value of sheet resistance. The $Al_xSi_yN_z$ passivated devices however show a smaller increase in drain resistance at higher drain current densities.

equivalent circuit model similar to the one used in this work (without the G_{GS} and G_{GD} parasitic conductances), determines a relation between the model elements and the intrinsic values of f_T and f_{MAX} by Equations 5.1 and 5.2, respectively.

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{5.1}$$

$$f_{MAX} = \frac{f_T}{\sqrt{4G_{DS}R_{in}(1+F)}} \tag{5.2}$$

where R_{in}, ω_T, and F are given by Equations 5.3, 5.4, and 5.5, respectively.

$$R_{in} = R_G + R_S + R_{GS} \tag{5.3}$$

$$\omega_T = 2\pi f_T \tag{5.4}$$

$$F = \frac{\omega_T L_S}{R_{in}} + \frac{2\omega_T C_{GD}}{G_{DS}}\left[1 + \frac{R_G}{R_{in}} + \frac{\omega_T L_S}{2R_{in}} + \frac{2\pi\tau}{C_{GS}R_{in}}\right] \tag{5.5}$$

As is obvious from these relations, f_T increased with available transconductance and is limited by the existence of gate-source and gate-drain capacitances. Shortening the gate length while maintaining a low aspect ratio between gate-length and barrier thickness has been shown to improve device transconductance, improving the measured f_T [17,134,137,141–143]. While capacitive loading presented by the dielectric passivation has been shown to decrease device f_T [8,44]. Device f_{MAX} is seen to be mainly limited by the device output conductance and input resistance. The addition of back-barriers to the HEMT epitaxial structure have been shown to decrease the output conductance of these devices [15], and T-gate style devices have been shown to decrease the gate resistance [137,144,145], both increasing the observed f_{MAX}.

Extrinsic f_T and f_{MAX}

For all device peripheries tested, f_T was found to optimize for L_G = 100 nm, while f_{MAX} was found to optimize for L_G = 200 nm. f_{MAX} was ~35% larger for devices with 100 μm vs. 250 μm periphery. Devices with 150 nm gates, and 100 μm periphery simultaneously yielded values of f_T and f_{MAX} close to (~10%) the maximum values measured on devices with L_G = 100 μm and L_G = 200 μm, respectively. Measured values of extrinsic f_T and f_{MAX} were ~10% larger for Si_yN_z passivated devices compared to $Al_xSi_yN_z$ passivated devices of the same dimensions, perhaps due to the slightly larger value of g_m measured for the Si_yN_z passivated devices indicated in 5.4. Representative extrinsic f_T and f_{MAX} values, along with values for key parasitics are recorded in Table 5.1 for devices with L_G=150 nm, so as to compromise between best f_T and f_{MAX}.

Intrinsic f_T and f_{MAX}

The intrinsic f_T and f_{MAX} values were obtained by de-embedding the pad capacitance values as described in a previous study [140]. It was found that the gate-drain pad capacitance (C_{PGD}) had the greatest impact on the f_{MAX}, while the gate-source (C_{PGS}) and drain-source (C_{PDS}) pad capacitance had a comparatively smaller effect. Table 5.2 records representative values of both intrinsic and extrinsic f_T and f_{MAX} as well as key parasitics for identically sized Si_yN_z and $Al_xSi_yN_z$ passivated devices. Aside from the pad capacitances, which would not be present in HEMTs incorporated into a MMIC, the key parasitics affecting f_T and f_{MAX} were found to be the R_G and output conductance G_{DS} for both the Si_yN_z and $Al_xSi_yN_z$ passivated devices. For the simple 2-layer epitaxial structure being used in this study, not much can be done to improve the output conductance of the fabricated HEMTs - as this parasitic mainly arises from leakage through the GaN buffer layer. Previous studies have shown that the output conductance can be greatly reduced with the use of an InGaN or AlGaN back-barriers [14,146,147], but epitaxial material of this type was not available for this study. Reduction of the gate resistance however, could be accomplished by the realization of devices with T-gates as described in many other studies [16]. T-gated devices provide a large cross section of metal for the gate, while minimizing parasitic gate capacitance by eliminating gate extensions toward the source and drain. These types of devices were not investigated as part of this study, as the fabrication of T-gates is considerably more difficult especially when utilizing a gate notch etch that requires a post etch anneal. Since the devices in this study were of the "vertical" gate type, as the gate length shrinks, so does the cross section of metal comprising the gate- resulting in a larger gate resistance for devices with shorter gate lengths. This was necessary to minimize the

parasitic capacitive loading that a larger gate overhang would produce. Table 5.2 lists the extrinsic f_T and f_{MAX} of two representative Si_yN_z and $Al_xSi_yN_z$ passivated devices along with values calculated from simulations where the values of the parastic elements are set to zero. As can be seen in the table, removal of the pad capacitance has a large effect on both f_T and f_{MAX}, but the removal of R_G and G_{DS} largely only affects f_{MAX}. It can be seen that very significant gains in f_{MAX} can be made by reducing both the gate resistance and output conductance. While the table shows simulated f_{MAX} values corresponding to reducing these parasitics to a value of zero, this would be impossible in reality - it only serves demonstrate the effect of these parasitics on f_{MAX}.

5.3.4 Large-Signal Measurement Setup

Large signal, load pull measurements were performed on a coplanar waveguide probing station set up with 250 μm pitch probes. The probes were connected to computer controlled tuners with an effective range of 1.8-18 GHz. 10 GHz CW generated by an HP3350B sweep oscillator were passed through a directional coupler and added to DC biasing from an HP4142B in a bias-T and passed though a computer controlled microwave tuner from Maury Microwave into a coplanar waveguide probe to the gate side of the device. Power meters monitored the microwave power input and reflected from the RF source at the directional coupler. The device was contacted on the drain side by coplanar waveguide probes connected to a narrow-band diplexer, which sends the fundamental and 2^{nd} harmonic components of the signal into two separate tuners. The fundamental signal passes through tuner and into a switched attenuator terminated with a power meter while the 2^{nd} harmonic (20 GHz) signal passes

Table 5.1: Extracted equivalent circuit elements extracted at 10 GHz for representative Si_yN_z and $Al_xSi_yN_z$ passivated HEMTs with W_G = 100 μm.

W_G = 100 μm, L_G = 0.15 μm L_{SG}= 0.35 μm, L_{GD} = 0.50 μm	Si_yN_z	$Al_xSi_yN_z$
C_{PGS}	15.2 fF	13.1 fF
C_{PGD}	13.3 fF	13.3 fF
C_{PDS}	20.8 fF	18.8 fF
L_G	23.8 pH	30.1 pH
L_S	3.9 pH	13.5 pH
L_D	14.3 pH	30.1 pH
R_G	32.9 Ω	26.8 Ω
R_S	6.9 Ω	6.5 Ω
R_D	10.0 Ω	9.6 Ω
R_{GS}	5.8 Ω	13.1 Ω
R_{GD}	10.6 kΩ	10.1 kΩ
C_{GS}	58.5 fF	68.1 fF
C_{GD}	0.7 fF	0.3 fF
C_{DS}	9.7 fF	10.4 fF
G_{DS}	1.03 mS	1.67 mS

Table 5.2: Extrinsic and Intrinsic (de-embedding of various parasitics) values of f_T, f_{MAX} for representative Si_yN_z and $Al_xSi_yN_z$ passivated devices with W_G = 100 μm and optimum f_{MAX}.

W_G = 100 μm, L_G = 0.15 μm	Si_yN_z		$Al_xSi_yN_z$	
L_{SG}= 0.35 μm, L_{GD} = 0.50 μm	f_T	f_{MAX}	f_T	f_{MAX}
Extrinsic	55 GHz	99 GHz	59 GHz	114 GHz
$C_{Pads} = 0$	87 GHz	212 GHz	89 GHz	200 GHz
$C_{Pads} = 0$, $R_G = 0$	87 GHz	486 GHz	89 GHz	444 GHz
$C_{Pads} = 0$, $R_G = 0$, $G_{DS} = 0$	89 GHz	549 GHz	91 GHz	507 GHz

through a tuner and into a power meter. Tuner positions were chosen to optimize either output power, efficiency, or gain of the measured HEMTs at various drain biases. The gate was typically biased at the quiescent point of maximum transconductance. A similar measurement setup for characterization at 35 GHz (but excluding the 2^{nd} harmonic tuning) was performed at Raytheon Integrated Defense Systems.

10 GHz Load-Pull Measurements

Measurements of P_{out} , G, and PAE with 10 GHz (CW) input power swept from -15 to 15 dBm at a drain bias of 35 V on identically sized Si_yN_z and $Al_xSi_yN_z$ devices are plotted in Figure 5.11.

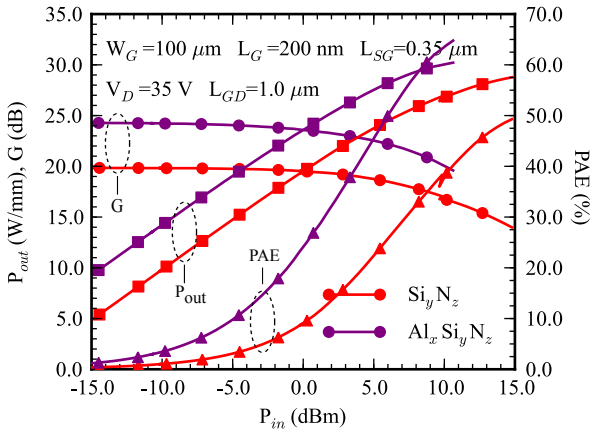

Figure 5.11: 10 GHz (CW) load-pull data taken with 35 V drain bias and microwave input power ranging from -15-15 dBm on a HEMT with W_G=100 μm, L_G=200 nm, L_{SG}=0.35 μm, and L_{GD}=1.0 μm. The $Al_xSi_yN_z$ show superior P_{out}, PAE, and G over their Si_yN_z counterparts. The larger value of G for the $Al_xSi_yN_z$ devices was likely due to the deeper gate recess these devices received. Measurements courtesy of Kat Harvard at Cornell University.

Tuner positions were chosen to maximize the device efficiency. By optimizing the 2^{nd} harmonic tuner, efficiencies as high as 82%, were measured on the $Al_xSi_yN_z$ passivated devices- indicating Class-C operation. The efficiency of the Si_yN_z passivated devices was found to be much lower than corresponding $Al_xSi_yN_z$ passivated devices, with the effect being more dramatic at the higher range of input power. Figure 5.12 plots the maximum values of P_{out}, PAE, and G resulting from similar power sweeps depicted in 5.11 at increasing drain bias.

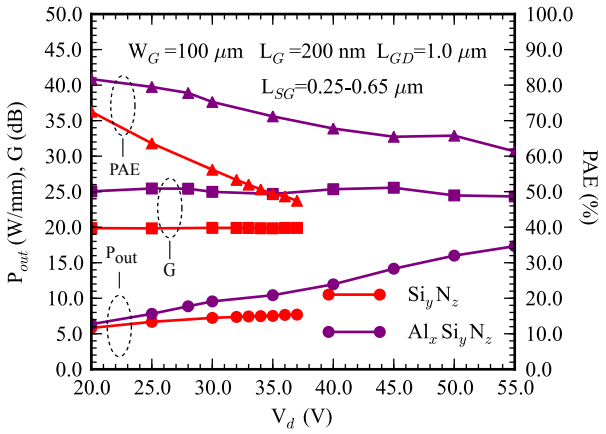

Figure 5.12: 10 GHz (CW) load-pull summary data taken with drain bias varying from 20-55 V on a HEMTs with W_G=100 μm, L_G=200 nm, L_{SG} ranging from: 0.25-0.65 μm, and L_{GD}=1.0 μm. This plot tabulates the maximum values of P_{out}, PAE, and G from power sweep measurements at fixed drain bias. Data for the Si_yN_z only extends to ~37 V, as this is where most of the devices failed due to breakdown. Measurements courtesy of Kat Harvard at Cornell University.

Data were collected on devices with L_G = 200 nm, L_{GD} = 1.0 μm, and W_G = 100 μm with the devices tuned for maximum efficiency. The value of L_{SG} varied across the whole range printed and was found to have little effect on any of the measured parameters. As can be seen in Figure 5.12, the $Al_xSi_yN_z$ passivated devices yielded higher PAE, gain, and output power density at all values of drain bias tested. The measured Gain was seen to have little dependence on drain bias, while PAE was shown to decrease with increased drain bias. The increased PAE seen in the $Al_xSi_yN_z$ devices as compared to the Si_yN_z devices is attributed to the reduction of electric fields in the gate-drain region, reducing electron injection to the surface of the device which leads to dispersion and reduced efficiency. The Si_yN_z passivated devices were unable to be biased beyond ~37 V on the drain, where they suffered breakdown. However, similarly sized

$Al_xSi_yN_z$ passivated devices could be biased to ~55 V - a 55% improvement. At 55 V on the drain, the $Al_xSi_yN_z$ passivated devices exhibited power densities 17.6 W/mm, which is the largest reported to date at this value of drain bias. As indicated in Figure 5.12, the power density was still increasing linearly with applied drain bias at the point of device breakdown - leading to the assumption that if larger values for L_{GD} were printed, larger power densities would have likely been possible. PAE as high of 82% was measured on the $Al_xSi_yN_z$ passivated devices at 20 V drain bias, which is the highest efficiency measured to date on an AlGaN/GaN HEMT and indicates class-C operation. The larger gain measured on the $Al_xSi_yN_z$ passivated devices was likely due to the increased g_m resulting from the deeper gate recess and the lack of nonlinear source resistance at high drain current density as compared to the Si_yN_z passivated devices.

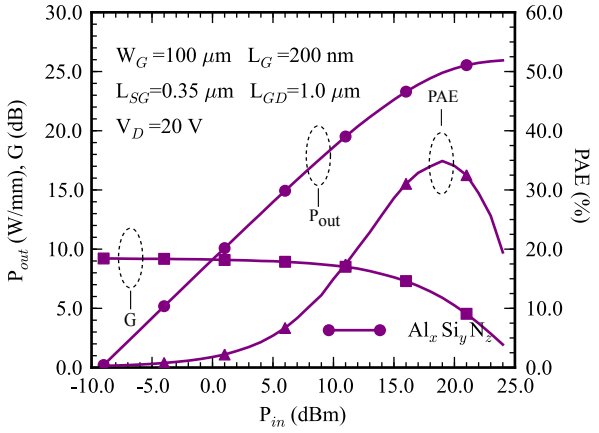

Figure 5.13: 35 GHz (CW) load-pull data taken with 20 V drain bias and microwave input power ranging from -10-25 dBm on an $Al_xSi_yN_z$ passivated HEMT with W_G=100 μm, L_G=200 nm, L_{SG}=0.35 μm, and L_{GD}=1.0 μm. Measurements were made with tuners optimized for maximum output power. Measurements courtesy of Raytheon Integrated Defense Systems, Andover, MA.

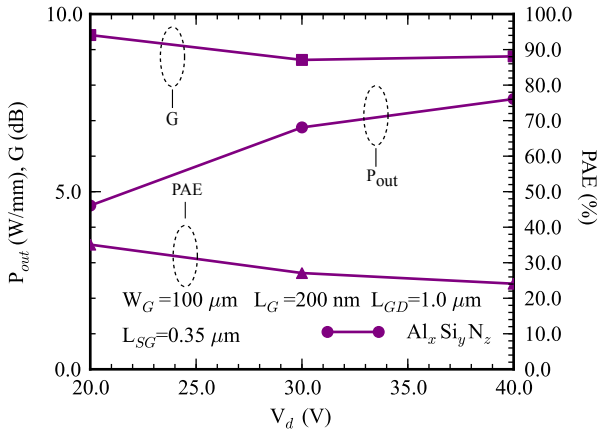

Figure 5.14: 35 GHz (CW) load-pull summary data taken with drain bias varying from 20-40 V on $Al_xSi_yN_z$ passivated HEMTs with W_G=100 μm, L_G=200 nm, L_{SG} ranging from: 0.25-0.65 μm, and L_{GD}=1.0 μm. The plot tabulates the maximum values of P_{out}, PAE, and G from power sweep measurements at fixed drain bias. Measurements were made with tuners optimized for maximum output power. Measurements courtesy of Raytheon Integrated Defense Systems, Andover, MA.

35 GHz Load-Pull Measurements

Load-pull data were also collected at 35 GHz (courtesy of Raytheon integrated defence systems), without the use of 2^{nd} harmonic tuning. Figure 5.13 depicts 35 GHz (CW) measurements of P_{out}, PAE, and G of an $Al_xSi_yN_z$ passivated HEMT with L_G = 200 nm, L_{GD} = 1.0 μm, and W_G = 100 μm, taken with 20 V on the drain and input power ranging from -10-25 dBm. Figure 5.14 plots the maximum values of P_{out}, PAE, and G resulting from similar power sweeps depicted in 5.13 at drain biases ranging from 20-40 V. With 20 V on the drain, maximum PAE and G measured 35% and 9.5 dB, respectively, and maximum Pout measured 7.6 W/mm with 40 V drain bias.

CHAPTER 6

GROUP-5 METAL BASED OHMIC CONTACTS TO THE ALGAN/GAN TWO-DIMENSIONAL ELECTRON GAS

6.1 Introduction

Building on prior work showing promising ohmic contact performance with the addition of Ta to the first layer of the Ti/Al/Mo/Au based metallization stacks of AlGaN/GaN HEMTs [148], a parametric study of the ohmic contact performance of several M/Ti/Al/Mo/Au metal stacks was explored where M represents one of the group-5 metals: V, Nb, and Ta. Thicknesses of 0, 75, 100, 125, and 150 Å of V, Nb, and Ta were explored as first-layer metals underneath a (150/900/400/500 Å) Ti/Al/Mo/Au metallization at activation temperatures ranging from 600-900°C on $Al_{0.25}Ga_{0.75}N$ heterostructures with ~25 nm barriers grown on both Al_2O_3 and SiC substrates as well as a sample with a 6.5 nm $Al_{0.40}Ga_{0.60}N$ barrier with a 2 nm GaN cap and a 1 nm AlN interbarrier.

6.2 Fabrication

Fabrication of transmission line method (TLM) structures on each of the $Al_{0.25}Ga_{0.75}N$ on sapphire, $Al_{0.25}Ga_{0.75}N$ on SiC, and $Al_{0.40}Ga_{0.60}N$ on SiC with AlN interbarrier began with the etching of 100 nm isolation mesas as described in Chapter 4. Samples were then cleaned and coated with 30 nm of Si_yN_z as described in Chapter 2. The samples were then coated with a bilayer of SPR955-0.9i/LOR3A and patterned with TLM patterns of 250 μm wide TLM structures

of 5, 10, 15, 20, 25, 30, 35, and 40 μm on the active mesa areas. The mask was used to etch the dielectric in a SF_6/Ar ICP-RIE process described in Appendix A and the remaining mask was used to lift off the ohmic metals in question. The samples were cleaned in 1:1 HCl:H_2O for 5 minutes prior to loading in the electron beam evaporator, which was then evacuated to a pressure ~3.5 x 10^{-7} Torr. It was found necessary to affix the samples to a large copper block with a Ag bearing high-vacuum grease to prevent the resist from burning when exposed to the flux of high melting point metals in this study. The unwanted metals were then lifted off in NMP and rinsed with deionized H_2O. Annealing was accomplished in a N_2 purged RTA with a graphite susceptor for 1 minute at temperatures ranging from 600-900°C. A similar ohmic contact study used a two-step annealing process [148], however, little rationale was given for this and it adds another variable to the experiment. Hence a single temperature, 1 minute annealing process was used. Samples were allowed to cool inside the RTA to below 200°C and then unloaded.

6.3 Measurement

Measurement of the ohmic contact properties were made by the 4 contact TLM method described in [149]. The plan-view of the TLM structure and probing setup are shown in Figure 6.1. The metal contacts are separated by increasing spacings labeled S1, S2, S3... etc. Measurements were made on a DC probe station driven by a HP4145A with 4 SMUs configured as follows: SMU 3 and SMU 4 are set to high-impedance mode, so that they do not source or sink any current. SMU 1 forces 20 mA into the top contact and SMU 2 is set to ground. Since SMU 3 and SMU 4 are set to high-impedance, all the current from SMU 1 must

be collected by SMU 2. The resistance between the two contacts is calculated from Equation 6.1.

$$R(\Omega) = \frac{V1 - V2}{I1} \tag{6.1}$$

The resistance between each of the contacts corresponding to spacings S1-S8 are tabulated and plotted as seen in Figure 6.2, as a function of spacing. A least squares linear fit is made to the data, the slope of which is used to calculate the sheet resistance (ρ_s) as in Equation 6.2, while the R intercept has a value equal to twice the contact resistance R_c, and the x intercept is equal to twice the transfer length (L_T). The specific contact resistivity ρ_c is then calculated as in Equation 6.3.

$$\rho_s(\Omega/\square) = \frac{dR}{dx}W \tag{6.2}$$

$$\rho_c(\Omega - cm^2) = R_c W L_T \tag{6.3}$$

6.4 X/Ti/Al/Mo/Au Survey on AlGaN/GaN/Al_2O_3

Initial experiments comparing the V, Nb, and Ta first layer metallizations to the the Ti/Al/Mo/Au (150/900/400/500 Å) only metallization were performed on $Al_{0.25}Ga_{0.75}N/GaN/Al_2O_3$ samples which had a 25 nm, 25% Al barrier layer. Plotted in Figures 6.3 and 6.4 are the contact resistance and specific contact resistivity, respectively, of the V, Nb, and Ta first layer metallizations of thicknesses 0, 75, 100, 125, and 150 Å after annealing at temperatures from 750-900°C. Data were taken at annealing temperatures as low as 600°C, but the contacts showed rectifying behavior below annealing temperatures of 750°C and were thus not included in these plots. Across all the samples in this study, a sheet resistance

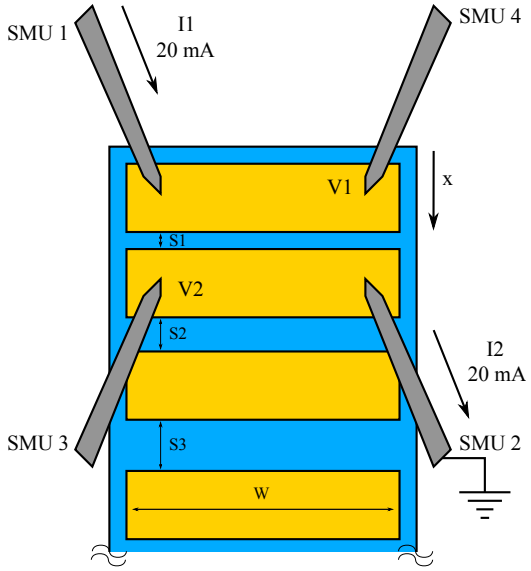

Figure 6.1: Measurement setup used to characterize the TLM structures fabricated in this study. Four SMUs are used: SMU 3 and SMU 4 are set to high-impedance voltage monitor mode and take or source no current. SMU 2 is set as a voltage ground while SMU 1 forces 20 mA into the top contact. As SMU 3 and SMU 4 are in high impedance mode, all the current from SMU 1 is collected in SMU 2. TLM contact spacings are indicated at S1, S2, S3... etc.

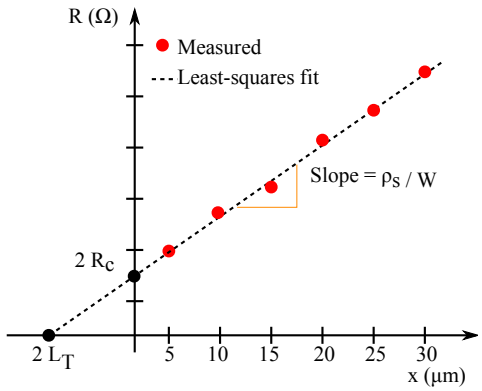

Figure 6.2: Graphical representation of collected TLM data. Contact resistance (R_c), transfer-length (L_T) and sheet resistivity (ρ_c) can be directly determined from the linear fit of the experimental data.

of ~475 Ω/□ was measured and its uniformity is reflected in the congruence of the R_c and ρ_c plots for all the metallizations. As is evident in Figures 6.3 and 6.4, the contacts containing 100 Å of V as the first layer and annealed at 850°C for 1 minutes showed the best performance in R_c and ρ_c, with values of 0.14 Ω-mm and 1.59 x 10^{-6} Ω-cm^2, respectively. The the transfer length on these samples measured 0.58 μm. The Ti/Al/Mo/Au only metallization showed almost the same performance when annealed at a lower temperature of only 800°C, but as will be shown later has a very rough surface morphology with poor edge acuity. The values of R_c and ρ_c for the Ti/Al/Mo/Au metallization are also seen to be much more temperature sensitive than the corresponding values for the V first layer metallization, which shows more of a flat response of these parameters with annealing temperature. The Ta first layer metallizations also optimized with a 100 Å Ta thickness and 850°C annealing with values of R_c and ρ_c values of 0.19 Ω-mm and 2.35 x 10^{-6} Ω-cm^2, respectively. The Nb first layer was shown to have the poorest performance and optimized at a thickness of 150 Å with 850°C annealing and had values of R_c and ρ_c values of 0.23 Ω-mm and 4.89 x 10^{-6} Ω-cm^2, respectively.

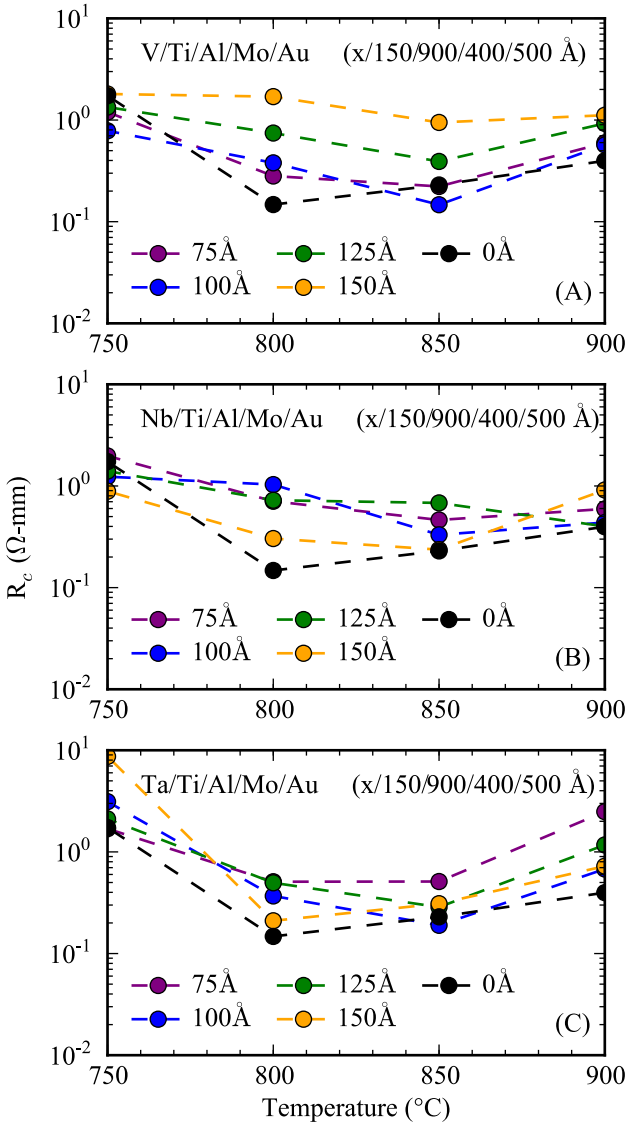

Figure 6.3: Plots of measured contact resistance R_c vs 1 minute annealing temperature for V/Ti/Al/Mo/Au (A), Nb/Ti/Al/Mo/Au (B), and Ta/Ti/Al/Mo/Au (C) metal stacks of thickness x/150/900/400/900 Å on samples grown on sapphire substrates. Also plotted in (A), (B), and (C) is a comparison with with a Ti/Al/Mo/Au stack of thickness 150/900/400/500 Å. Minimum contact resistance was found to be 0.14 Ω-mm on samples containing a 100 Å V layer and 1 minute annealing at 850°C.

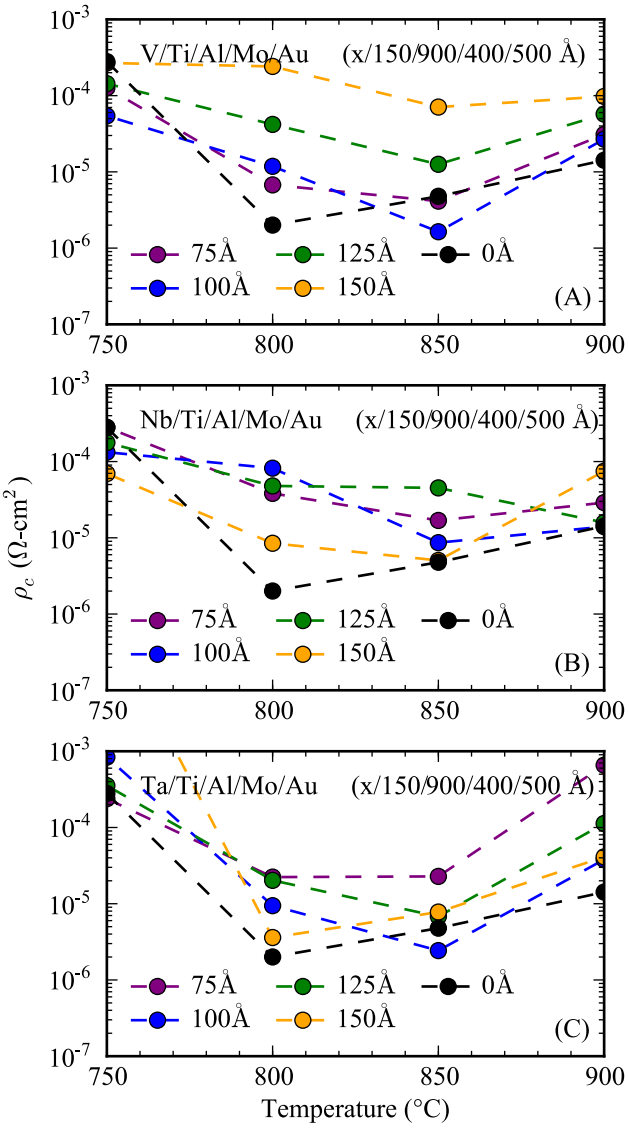

Figure 6.4: Plots of measured specific contact resistivity (ρ_c) vs 1 minute annealing temperature for V/Ti/Al/Mo/Au (A), Nb/Ti/Al/Mo/Au (B), and Ta/Ti/Al/Mo/Au (C) metal stacks of thickness x/150/900/400/900 Å on samples grown on sapphire substrates. Also plotted in (A), (B), and (C) is a comparison with with a Ti/Al/Mo/Au stack of thickness 150/900/400/500 Å. Minimum ρ_c was found to be 1.58 x 10^{-6} Ω-cm^2 on samples containing a 100 Å V layer and 1 minute annealing at 850°C.

A possible reason for the high performance of the V first layer metallizations may be indicated in Table 6.1, which records the metal work function (ϕ_m), enthalpy of formation of the most stable metal nitride (H_f (MN)), and the work function of the most stable metal nitride (ϕ_{MN}) with values taken from [59,150–154]. For a V/Ti/Al/Mo/Au based metallization, the H_f of VN would indicate that it is less likely to form than TiN, but due to the fact it is the first layer of the metallization, it may have a chance to react with the AlGaN before the Ti diffuses to the AlGaN interface. Also evident is the much reduced work function of VN compared to TiN which would contribute to a lowered barrier height on the AlGaN surface compared to the other metal nitrides. All the other group-5 metal nitrides explored in this study have larger work functions than TiN, which could be a possible reason for their reduced performance compared to the V first layer metallizations.

Table 6.1: Table indicating the work function ϕ_m, enthalpy of formation H_f for most stable metal nitride, and the melting point of the first-layer metals explored in this ohmic contact study.

Metal	ϕ_m (eV)	H_f (MN) (kJ/mol)	ϕ_{MN} (eV)
Ti	4.33	-168	3.74
V	4.30	-93	3.56
Nb	4.36	-134	3.92
Ta	4.25	-128	4.00

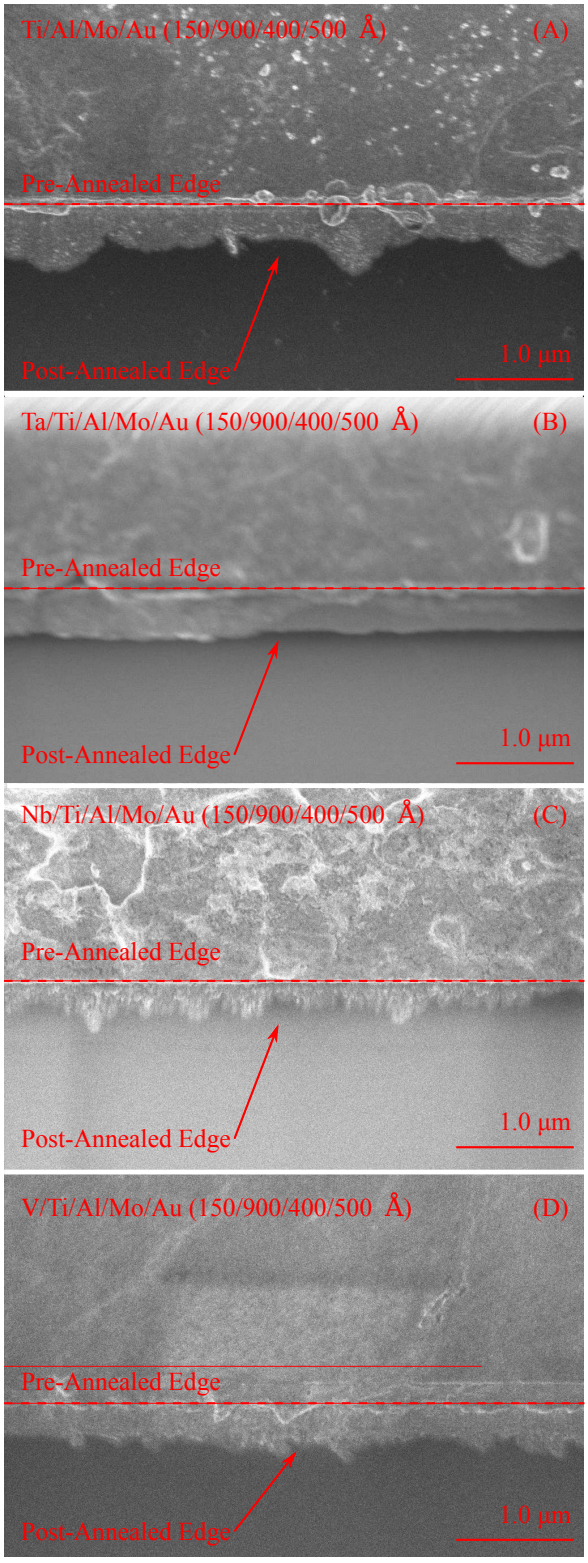

Figure 6.5: Plan-view SEM images of the 850°C/1 min annealed Ti/Al/Mo/Au (A), Ta/Ti/Al/Mo/Au (B), Nb/Ti/Al/Mo/Au (C), V/Ti/Al/Mo/Au (D) metallizations.

Figure 6.5 shows plan view SEM images of the Ti/Al/Mo/Au (A), Ta/Ti/Al/Mo/Au (B), Nb/Ti/Al/Mo/Au (C), and V/Ti/Al/Mo/Au (D) post 850°C annealing for 1 minute. Evident in all these images are the rough surfaces and poor edge definition of contacts. Rough surfaces do not necessarily harm HEMT performance but poor edge definition can result in the source/drain contacts shorting to the gate metallization, rendering the device useless. It has been proposed in literature and discussed in Chapter 1 that the poor edge definition Ti/Al/Mo/Au based contacts arises from the Au and Al diffusing together during anneal. Au and Al are known to form a low temperature eutectic composition which the flowing is reportedly a result of.

6.5 X/Ti/Al/Mo/Au on AlGaN/GaN/SiC

As evidenced in the above section, Au overlayers yielded the lowest values of R_c and ρ_c. Hence an additional experiment was performed to see how X/Ti/Al/Mo/Au metallizations performed on state-of-the-art device quality material consisting of $Al_{0.25}Ga_{0.75}N$/GaN/SiC with 25 nm barriers. V/Ti/Al/Mo/Au, Nb/Ti/Al/Mo/Au, and Ta/Ti/Al/Mo/Au (100/150/900/400/500 Å) were deposited as before and the samples annealed in the 775-900 °C temperature range. The results of the measurement of R_c and ρ_c are recorded in Figure 6.6. The V and Ta first-layer metallizations were found to have the lowest values of R_c and ρ_c when annealed at 850 °C. The Ta first-layer sample technically yielded the best performance with R_c=0.15 Ω-mm and ρ_c=2.02 x 10^{-6} Ω-cm^2, while the V first-layer sample yielded results that were close with R_c=0.18 Ω-mm and ρ_c=2.52 x 10^{-6} Ω-cm^2. The values of the V based sample were, like before, less temperature sensitive than the corresponding Ta

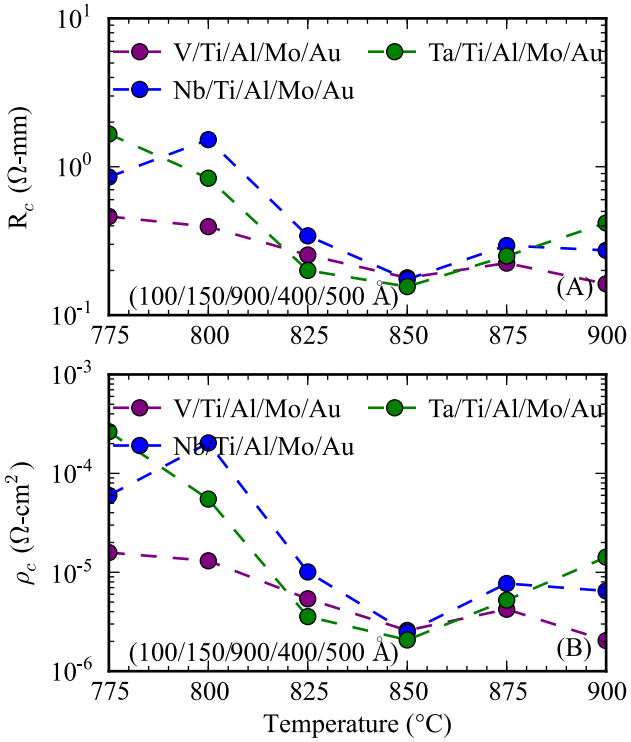

Figure 6.6: Plots of measured contact resistance (R_c) (A), and specific contact resistivity (ρ_c) (B), for V/Ti/Al/Mo/Au, Nb/Ti/Al/Mo/Au, and Ta/Ti/Al/Mo/Au metal stacks of thickness 100/150/900/400/500 Å on samples grown on S.I. SiC substrates vs. 1 minute annealing temperature.

based samples- showing a flatter response allowing for a wider processing window of anneal temperature.

6.6 X/Ti/Al/Mo/Au on GaN/AlGaN/AlN/GaN/SiC

As ohmic contact formation on HEMT samples containing a high Al percentage in the barrier and an AlN interbarrier has historically been difficult, an additional experiment was performed to see how the X/Ti/Al/Mo/Au metallizations performed on device quality material consisting of GaN/$Al_{0.40}Ga_{0.60}N$/

AlN/GaN/SiC with 6.5 nm barriers, 2 nm GaN caps and a 1 nm AlN interbarrier. V/Ti/Al/Mo/Au, Nb/Ti/Al/Mo/Au, and Ta/Ti/Al/Mo/Au (100/150/900/400/500 Å) were deposited as before and the samples annealed in the 775-900 °C temperature range. The results of the measurement of R_c and ρ_c are recorded in Figure 6.7. The V and Ta first-layer metallizations were again found to have the lowest values of R_c and ρ_c when annealed at 850 °C. The Ta first-layer sample again technically yielded the best performance with R_c=0.21 Ω-mm and ρ_c=2.02 x 10^{-6} Ω-cm^2, while the V first-layer sample yielded results that were close with R_c=0.22 Ω-mm and ρ_c=4.36 x 10^{-6} Ω-cm^2. The values of the V based sample were, like before, less temperature sensitive than the corresponding Ta based samples- showing a flatter response allowing for a wider processing window of anneal temperature.

6.7 X/Ti/Al/Mo/Y on AlGaN/GaN/Al_2O_3

As discussed in Chapter 1, a corrosion resistant overlayer serves to reduce the ohmic contact resistance by protecting the underlying metals from oxidizing and becoming resistive. As described in Chapter 1, overlayers of Au are the most popularly reported in literature, as they are both corrosion resistant and highly conducting. A recent study exists where Ag is employed for the same effect, utilizing a V/Al/V/Ag stack [155]. Low contact resistivity and good edge definition were achieved, the latter was attributed to the elimination of the possibility of of the well published Au-Al eutectic that results in the lateral flowing of the metallization. However as recorded in Table 6.2 it is seen that the Ag-Al system actually has an even lower eutectic point than that of the Au-Al system, so it is unlikely that this was the reason for the observa-

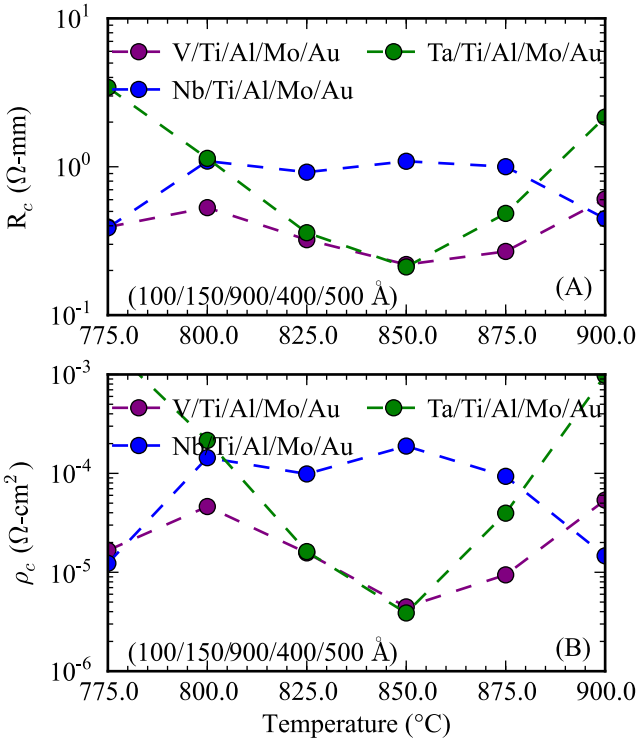

Figure 6.7: Plots of measured contact resistance (R_c) (A), and specific contact resistivity (ρ_c) (B) vs. 1 minute annealing temperature, for V/Ti/Al/Mo/Au, Nb/Ti/Al/Mo/Au, and Ta/Ti/Al/Mo/Au metal stacks of thickness 100/150/900/400/500 Å on samples containing a 1 nm AlN interbarrier between the AlGaN barrier and GaN buffer.

tion of reduced edge roughness. No study to date has attempted to employ Cu for the upper layer, however it has the highest melting point compared to that of Au or Ag, is more conductive than Au, and has the same valence. A comparison was desired between the X/Ti/Al/Mo/Au metallizations discussed above with X/Ti/Al/Mo/Y metallizations, where X again represents V, Nb, or Ta, and Y represents Cu, Ag, or Au. 100 Å of the group-5 metal was chosen as the first layer and 500 Å of either Cu, Ag, or Au as the overlayer. The metallizations were prepared as before and annealed from 775-900 °C for 1 minute. Plotted in Figure 6.8 are the results of this experiment, with

Table 6.2: List of melting point (T_m), Al-Metal eutectic temperature (T_{eu}), and resistivity (ρ), of the metal overlayers explored in this study.

Metal	T_m (°C)	T_{eu} Al-Metal (°C)	ρ (nΩ-cm)
Cu	1084.6	548	16.8
Ag	961.8	567	15.9
Au	1064.2	650	22.1

the measured values of R_c for Cu overlayers (A), Ag overlayers (B) and Au overlayers (C) shown. V based contacts universally measured the lowest values of R_c, with V/Ti/Al/Mo/Cu, V/Ti/Al/Mo/Ag/, and V/Ti/Al/Mo/Au yielding 0.28 Ω-mm at 850 °C, 0.25 Ω-mm at 800 °C, and 0.14 Ω-mm at 850 °C. While the Au overlayers were the highest performing, the values of R_c for the Cu and Ag overlayers were certainly usable for HEMTs, comparing favorably to other common metallizations in previous studies. The most interesting difference between the V/Ti/Al/Mo/Y contacts was the edge definition after annealing. SEM images in Figure 6.9, show plan-view scans of 850 °C annealed ohmics of V/Ti/Al/Mo/Cu (A), V/Ti/Al/Mo/Ag (B), and V/Ti/Al/Mo/Au (C) at equal magnifications. It is evident that the Cu and Ag terminated metallizations show superior edge definition when compared to the Au capped one. With the Cu capped metallization exhibiting no flow beyond the lithographically defined metal edge post anneal.

6.8 PECVD Si_yN_z Encapsulation of Ohmic Metals

While the Cu overlayer based ohmic contact schemes exhibited no lateral flowing post anneal, their resistance was higher than the Au overlayer based

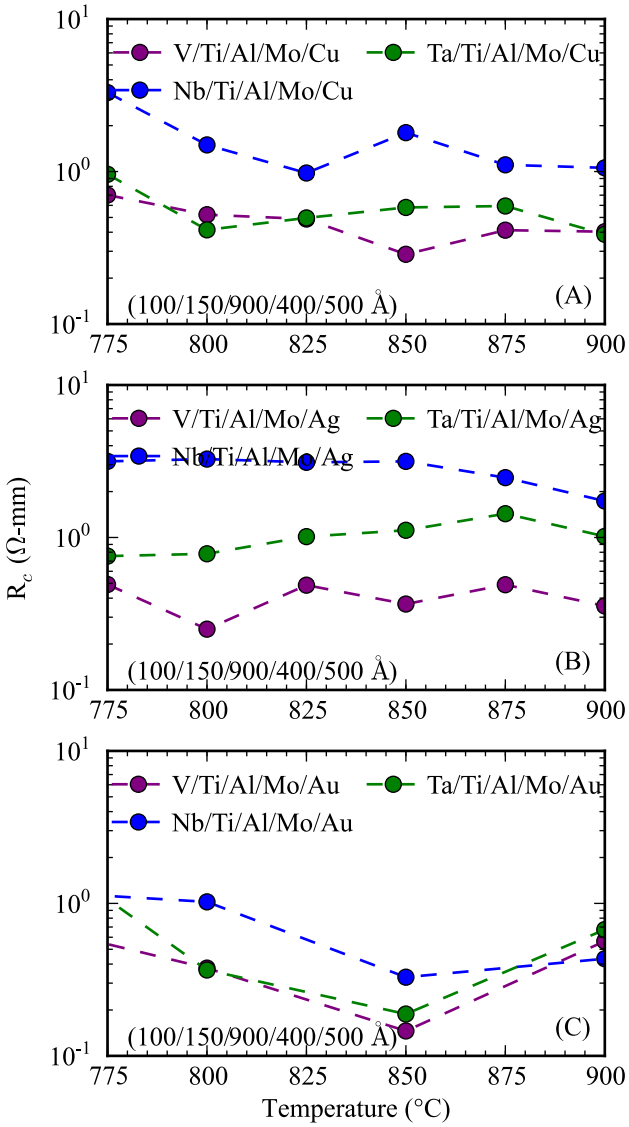

Figure 6.8: Plots of measured contact resistance (R_c) vs 1 minute annealing temperature for V/Ti/Al/Mo/x, Nb/Ti/Al/Mo/x, and Ta/Ti/Al/Mo/x metal stacks of thickness 100/150/900/400/500 Å on samples grown on sapphire substrates where x represents Cu (A), Ag (B), and Au (C). Au overlayers and V underlayers universally provided the best performance in R_c.

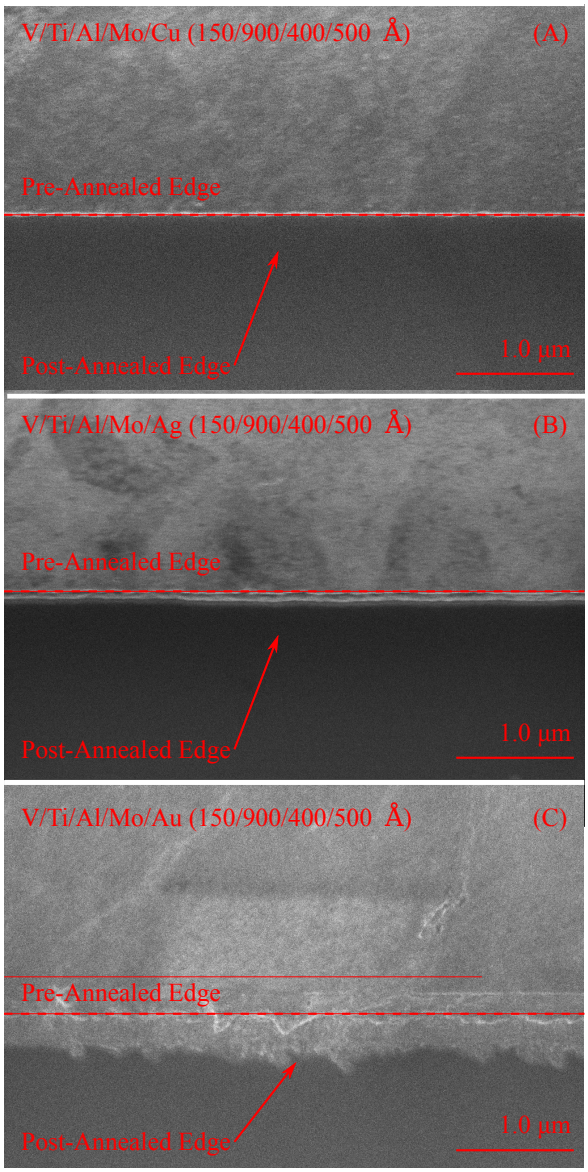

Figure 6.9: Plan-view SEM images comparing V/Ti/Al/Mo/Cu (A), V/Ti/Al/Mo/Ag (B), V/Ti/Al/Mo/Au (C) metallizations post 850°C/1 minute anneal. The Cu overlayer resulted in the smoothest contact with the best edge definition, while the Au overlayer yielded the roughest contact with a large degree of lateral ohmic flow post anneal. The Ag overlayer resulted in a rough contact surface but minimal lateral flow.

schemes. An attempt was made to contain the Au containing ohmic metals during anneal with a refractory dielectric that could later be etched away to expose the ohmic regions when it came time to make pad connections. As discussed in Chapter 1, a couple of different encapsulation schemes have been published in the past with some success, but often resulted in the encapsulation cracking and releasing the melted metal inside or a degradation of the contact electrical properties. As it was overall the best performing contact in this study, the V/Ti/Al/Mo/Au stack was applied to the $Al_{0.25}Ga_{0.75}N$ material described earlier and PECVD deposited Si_yN_z encapsulation was attempted to contain the metallization. As there was a concern of cracking as described in a previous study [83], the Si_yN_z was kept very thin at just slightly thicker than what would be needed for a nearly pinhole free film (~30 nm). In anticipation of there being problems with cracking "relief" holes were lithographically patterned over some of the metal contact areas and the Si_yN_z selectively removed by a CHF_3/O_2 RIE as detailed in Appendix A. Some metal contacts were however left totally encapsulated. A cross-sectional schematic of this process is detailed in Figure 6.10. The contact was annealed with the encapsulation in place at the optimum anneal temperature of 850 °C for 1 minute and the sample inspected. No cracking of the Si_yN_z film was observed over the contacts containing relief holes or ones without such reliefs. After stripping the Si_yN_z in another CHF_3/O_2 etch (so the metal edges would be exposed) the sample was inspected in the SEM and the plan view images at two different magnifications are shown in Figure 6.11. It is obvious from the SEM image that the scheme was successful and no lateral flow of the contact occured as in Figure 6.5 (D), which was of the same metal composition annealed in the same way without the encapsulation. A comparison of measurements of R_c and ρ_c for encapsulated vs. unencapsulated schemes

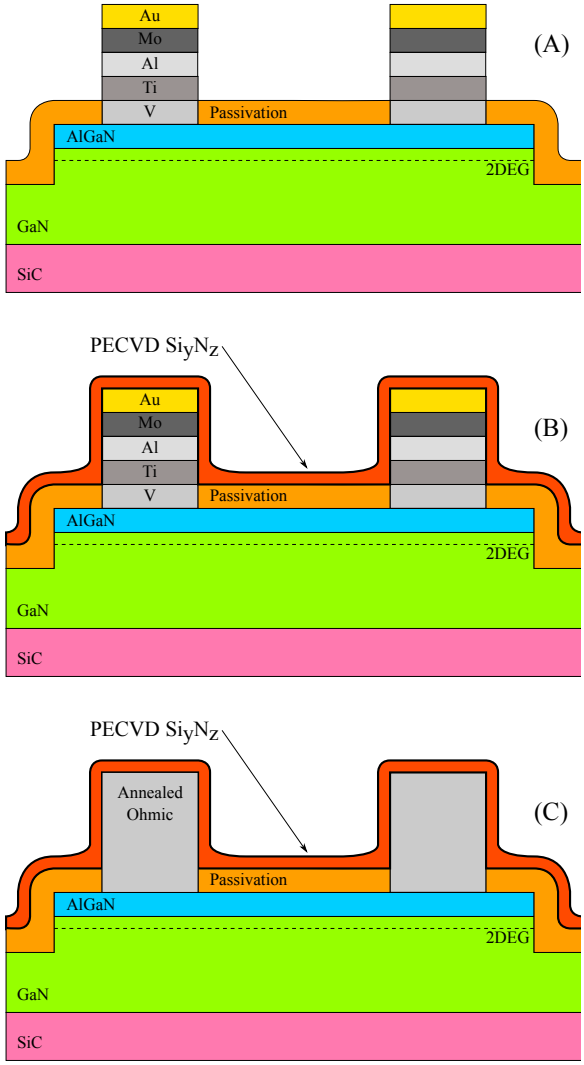

Figure 6.10: Cross-sectional schematic of PECVD Si_yN_z encapsulation process to contain the ohmic metal during anneal. After source/drain windows are etched and ohmic metal is lifted-off (A), 30-35 nm of PECVD Si_yN_z is deposited on the entire sample (B). When the ohmic metal undergoes RTA annealing at the activation temperature (C) it is contained by the PECVD Si_yN_z encapsulation, preventing flow.

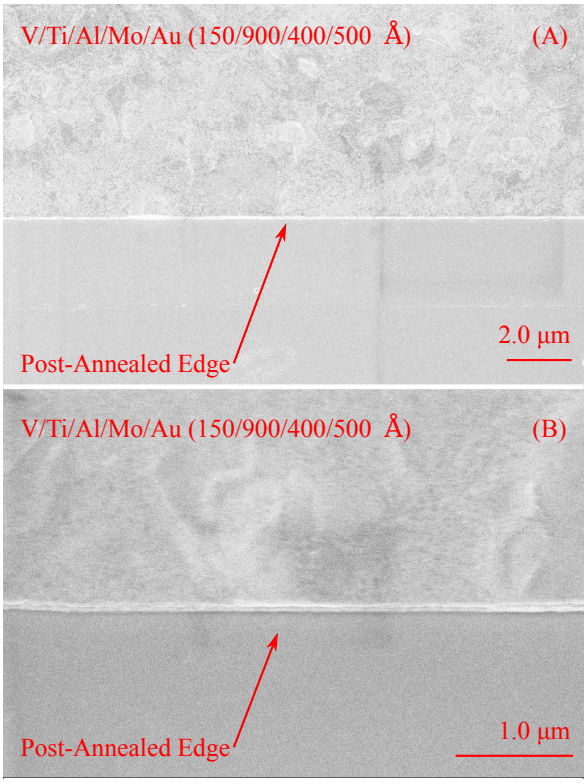

Figure 6.11: Plan-view SEM images of V/Ti/Al/Mo/Au ohmics annealed at 850°C for 1 min while encapsulated in 30-35 nm of PECVD Si_yN_z. In these images the PECVD Si_yN_z has been removed via CHF_3/O_2 RIE plasma so that the metal edge could be investigated.

revealed that the encapsulation process did not adversely affect the electrical performance of the contact as performance metrics were within a very small margin of error (~5%).

CHAPTER 7

CONCLUSIONS AND FUTURE DIRECTIONS

7.1 Conclusions

7.1.1 Film Growth

It was effectively shown that composite films of Al_xN_z and Si_yN_z can be grown by LPCVD utilizing standard tooling with slight modifications to include an organometallic aluminum source. The addition of TMAl flux into a gas chemistry that normally only precipitates Si_yN_z results in a $Al_xSi_yN_z$ film with a growth rate much higher than that of the silicon nitride or aluminum nitride alone. It is also shown that the increase in growth rate saturates with increasing vapor aluminum mole fraction above 0.025. This increase in growth rate allows films of significant thickness to be grown at relatively low growth temperatures. Film composition measurements by RBS and XPS show a positive correlation of precursor aluminum vapor mole fraction with measured film aluminum mole fraction which like the growth rate, also saturates around a vapor mole fraction of 0.025 for the growth conditions studied. The XPS measurements detected a large impurity concentration of oxygen and carbon on the grown films but the RBS measurements show a lack of such impurities, leading to the conclusion that the impurities were only present on the surface of the films. HFS measurements show a low (3.5%) atomic concentration of incorporated hydrogen in the as-deposited film which is confirmed by the FTIR measurements that also showed the presence of hydrogen in the as-grown films. FTIR measurements on the films before and after short (30 second), high temperature (800°C

to 1100°C) rapid thermal anneals show that the hydrogen content can be significantly reduced by such treatment. Spectroscopic ellipsometry revealed that the composite film exhibits a dispersion characteristic intermediate to that of the silicon nitride or aluminum nitride alone - Leading to the conclusion that the bandgap of the film is higher than that of the silicon nitride, which was a goal of this study. The annealing of the films at high temperature in nitrogen was also shown to both decrease the film thickness and increase the film index of refraction, indicative of hydrogen removal and film densification.

7.1.2 AlGaN/GaN Heterostructure Passivation

C-V and XRD measurements of Si_yN_z and $Al_xSi_yN_z$ passivated AlGaN/GaN heterostructures resulted in the observation of a negative fixed charge at the passivation/AlGaN interface for the case of the $Al_xSi_yN_z$ passivation, while the Si_yN_z passivation was found to provide a slightly positive fixed charge at the same interface. A model adapted from a previously accepted study was used to calculate the magnitudes of the fixed charges at the passivation/AlGaN interface for both the Si_yN_z and $Al_xSi_yN_z$ passivations, finding that the the $Al_xSi_yN_z$ passivation contained a trapped sheet charge on the order of ~1.57 x $10^{12}cm^2$. XRD measurements confirmed the fixed charge was not originating from stress in the AlGaN barrier, as no shift in the AlGaN peak relative to the GaN peak was measured for any dielectric thickness or type explored. Dielectric permittivities for both Si_yN_z and $Al_xSi_yN_z$ were estimated from C-V measurements, confirming VASE data taken in Chapter 2 which indicated the $Al_xSi_yN_z$ had a reduced refractive index compared to Si_yN_z. These findings had large implications for AlGaN HEMTs fabricated using the two types of passivation as it was found

that the inclusion of negative interface charge at the passivation/AlGaN interface and the resulting lower concentration in the 2DEG was actually beneficial to device operation- it improved almost all device performance metrics explored, yielding devices with the current state-of-the-art efficiencies and low drain-bias power density.

7.1.3 High Electron Mobility Transistor Fabrication

A simple, hybrid electron-beam and photolithography based process was developed to evaluate HEMTs fabricated with an LPCVD passivation. The process utilized a unique harmasking step for the definition of the gate which allowed gate windows to be realized on the order of 50 nm and etched into the highly etch resistant $Al_xSi_yN_z$. The source and drain definition process was a self-aligned one, allowing the dielectric etch and lift-off step to be performed with the same level of lithography. This reduces the minimum spacing the source and gate metallizations can have with the gate metallization, which allows the reduction of access resistances in HEMT devices. A field plate gate process was used for simplicity, and high-temperature annealing was utilized prior to the gate-metal deposition. The high-temperature anneal step was found to be necessary to remove the etch products left behind from the $SF_6/BCl_3/Ar$ etch process used to define the gate window.

7.1.4 LPCVD Passivated AlGaN/GaN High Electron Mobility Transistors

Si_yN_z and $Al_xSi_yN_z$ passivations were integrated into a high electron mobility transistor fabrication process, and devices with both types of passivations evaluated in DC, small-signal, and large-signal test environments. The $Al_xSi_yN_z$ passivated devices showed much improved device performance metrics compared to their Si_yN_z counterparts, showing a reduced parasitic pad-capacitance and nonlinear source access resistance, and increased power density and efficiency at 10 and 35 GHz large signal operation.

7.1.5 Ohmic Contacts the the AlGaN/GaN Heterostructure

Several different ohmic contact schemes to AlGaN/GaN based heterostructures were investigated. An exploration on the dependence of contact resistance on V-group first-layer modifications to the standard Ti/Al/Mo/Au metallization resulted in ohmic contacts with excellent performance and a wide processing window. V and Ta based x/Ti/Al/Mo/Au metallizations were found to be the highest performing, with V providing a more lenient control on the annealing temperature used. The problem of lateral flow of the ohmic metals post annealing was addressed by encapsulating them in a thin PECVD Si_yN_z layer during anneal. No cracking of this film during anneal was noted, and it was found to have minimal effect on the electrical properties of the contact. Contacts annealed in this way showed very straight and smoothly defined ohmic contact edges post anneal. Alternative capping layers to Au were also investigated, it was found that V/Ti/Al/Mo/Y based metallizations with Y being a Ag or Cu

layer showed an increased but comparable contact resistance compared to metallizations with a Au overlayer. These metallizations were however effective in reducing the lateral flow and consequent edge roughness of the contacts post anneal.

7.2 Future Directions: Doped Field Plates

As was discussed, the ability to controllably deplete the 2DEG of the AlGaN/GaN HEMT channel while still tying up the surface states that exist at the AlGaN surface is crucial to realizing high-frequency high-power transistors with good efficiency. The $Al_xSi_yN_z$ films accomplished this task by not providing as much positive charge at the AlGaN/dielectric interface as the Si_yN_z did, thereby leaving this interface with a net negative charge. However, p-type doping a thin region at the surface of the AlGaN layer would provide the same effect; the ionized acceptors would create a fixed negative space charge in the doped region. Magnesium, although it has been shown to have a relatively high ionization energy [], and problems with hydrogen passivation [], is the most common p-type dopant for the AlGaN semiconductors. Due to its relatively high vapor pressure [], it is impractical to achieve p-type regions in AlGaN by high-temperature diffusion of metallic magnesium into the lattice. Ion implantation is also ruled out due to the damage is causes to the crystal [], and the high-temperatures required for AlGaN to anneal out such damage [].

One possible method of introducing magnesium into the surface of the AlGaN is to grow a dielectric containing significant amounts of magnesium ($Mg_xSi_yN_z$) on top ofthe heterostructure surface, and then anneal the resulting

stack at high temperature. The dielectric would protect the AlGaN from losing nitrogen during the anneal, and the magnesium it contained would be allowed to diffuse into the AlGaN surface. As long as the magnesium was incorporated into the crystal and not passivated by hydrogen, it would act as an acceptor and the ionized portion of these acceptors would create a negative space charge near the surface of the AlGaN. Additionally, the dielectric could be left in place to act as a passivation layer, which would mitigate DC-to-RF dispersion as discussed previously. Hence both the passivation of the structure and the addition of negative charge at the AlGaN/dielectric interface would be achieved in this way. Also, unlike the $Al_xSi_yN_z$ approach where the amount of fixed negative charge at the AlGaN/dielectric interface cannot be controlled easily, the $Mg_xSi_yN_z$ approach could achieve this control by varying the anneal parameters to control how much magnesium is introduced into the AlGaN surface.

7.2.1 Growth of $Mg_xSi_yN_z$

An investigation into the feasibility of synthesizing $Mg_xSi_yN_z$ was carried out in a manner similar to that of the synthesization of $Al_xSi_yN_z$ described in Chapter 2, with identical equipment, but by replacing the room-temperature TMAl bubbler with a heated Cp_2Mg bubbler to provide Mg flux. It was observed that to obtain an appreciable concentration of Mg in the grown films that the dichlorosilane flow had to be reduced significantly compared to the studies presented in Chapter 2, as the vapor pressure and subsequently the flux of Mg out of the bubbler is much smaller compared to that out of the Al out of the TMAl bubbler. The Cp_2Mg bubbler was kept at a pressure of 80 Torr, and a temperature of 50 °C. Utilizing dichlorosilane and ammonia flows, in addition to 90 sccm of

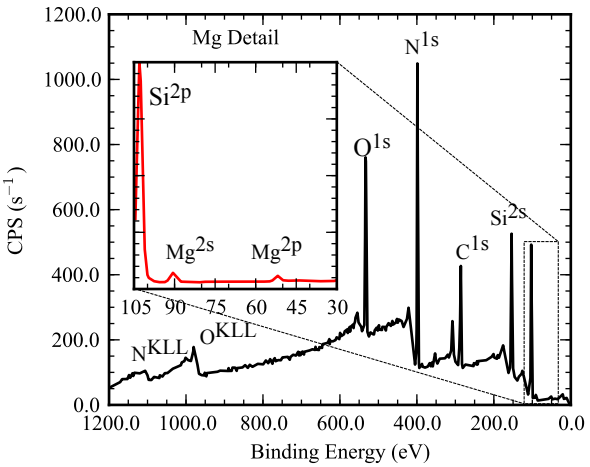

Figure 7.1: An XPS scan of a representavie $Mg_xSi_yN_z$ film as-grown. Analysis of this data reveals the Mg concentration in the film was ~3.4% by atomic %.

N_2 through the Cp_2Mg bubbler similar to what was used to grow pure Si_yN_z resulted in no detectable Mg content in the film by XPS. However, dropping the flow to 25 sccm, instead of 104 sccm, did result in detectable Mg spectral features in an XPS scan as seen in figure 7.1, but the growth rate of the film was reduced by a proportional amount compared to the growth of Si_yN_z.

7.2.2 Mg Diffusion from $Mg_xSi_yN_z$

AlGaN/GaN heterostructures consisting of 25 nm barrier layers of ~25% Al content were first profiled via Hg probe C-V. Thin (~30 nm) $Mg_xSi_yN_z$ films were then applied to AlGaN/GaN heterostructures at a growth temperature of 750 °C. Upon cooling the samples were subjeted to high temperature N_2 annealing in an RTA for times up to 5 minutes. The $Mg_xSi_yN_z$ was stripped in HF acid and the structure profiled again via Hg probe C-V. Figures 7.2 and 7.3 show the

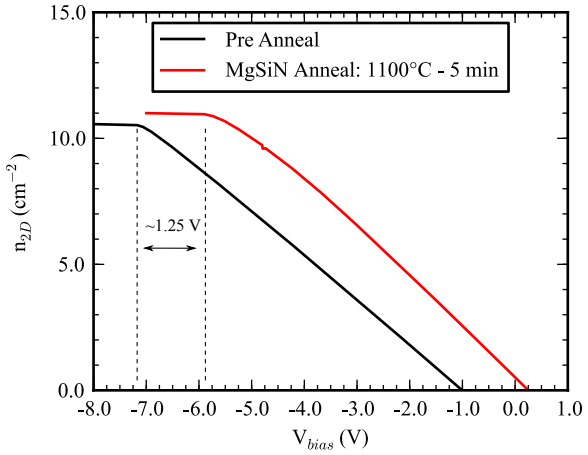

Figure 7.2: n_{2D} measurement by Hg probe C-V profiling of a bare AlGaN/GaN heterostructure before and after high temperature annealing in the presence of $Mg_xSi_yN_z$.

results of the Hg probe C-V profiling for both n_{2D} and n_{3D}, respectively, both before and after the above described treatment. As is evident from Figure 7.2, the treatment caused a 1.25 V shift in pinchoff voltage in the heterostructure, indicative of adding a layer of negative charge at the surface. Figure 7.3 provides further evidence to this fact, showing that the 2DEG density has shifted by around 3.25 nm as a result of the treatment. As direct evidence of Mg diffusion into the AlGaN, Figure 7.4 shows the results of a secondary ion mass spectrometry scan performed on a treated sample. These data show that the treatment described resulted in sucessful Mg diffusion into the sample to a depth of a few nanometers, which was similar to what was indicated by the C-V measurement shown in Figure 7.3.

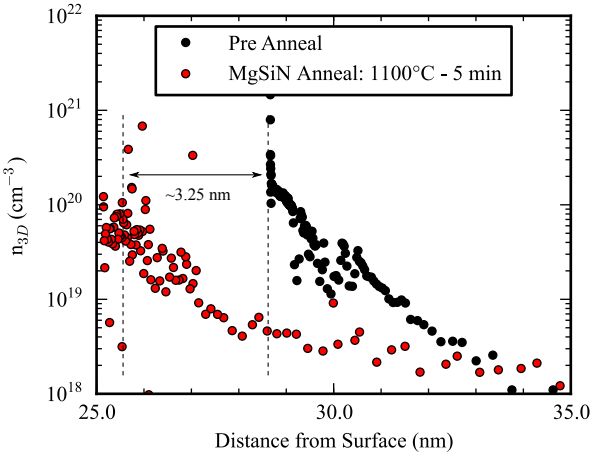

Figure 7.3: n_{3D} measurement by Hg probe C-V profiling of a bare AlGaN/GaN heterostructure before and after high temperature annealing in the presence of $Mg_xSi_yN_z$.

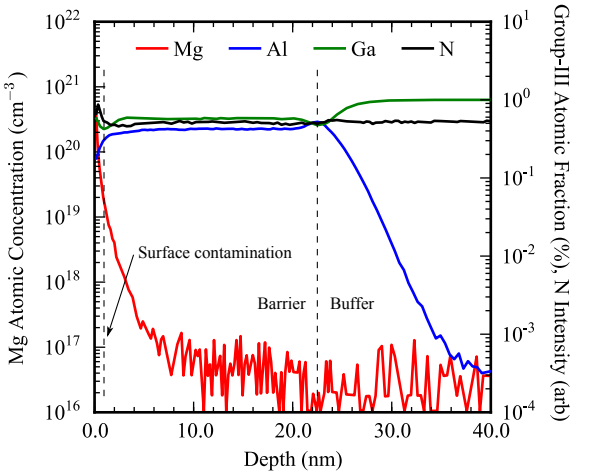

Figure 7.4: Results of secondary ion mass spectroscopy at depths ranging from 0 to 40 nm into the treated sample post dielectric strip. These results show successful Mg diffusion into the AlGaN layer.

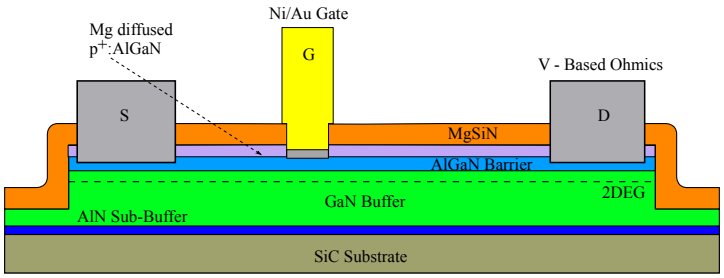

Figure 7.5: Proposed doped field plate device utilizing the $Mg_xSi_yN_z$ as both the passivation and the Mg diffusion source.

7.2.3 Proposed Doped Field Plate HEMT

As previously mentioned, the p-doped AlGaN surface layer will act as a field plate due its negative space charge. The $Mg_xSi_yN_z$, if left present after the difusion anneal, would also potentially act as an effective passivation. A proposed device fabricated with in this manner is depicted in Figure 7.5. Measurements of the index of refraction of $Mg_xSi_yN_z$ by VASE (shown in Figure 7.6) have shown that it has an infared index of refraction even lower than that of the $Al_xSi_yN_z$, and just slightly greater than what was measured for the AlN films in this study. By similar arguments made in Chapter 3, these data point to the $Mg_xSi_yN_z$ films having a smaller permittivity than the $Al_xSi_yN_z$ that were previously discussed; this would present a smaller parasitic capacitancitve loading in a fabricated device. However, depleting the channel uniformly between source and drain could cause problems with increased access resistance. Selectively depleting the channel in the vicinity of the gate terminal would likely give the best performance as this is where the large electric field exists, and depleting the whole channel will just increase the sheet resistance. By first depositing Si_yN_z, then opening a window in it centered on the gate region, the $Mg_xSi_yN_z$ could then be deposited in this opening. Annealing this structure at high temperature

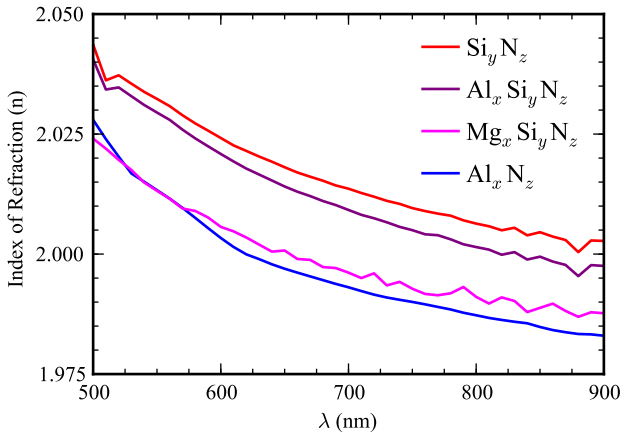

Figure 7.6: VASE data comparing the index of refraction of $Mg_xSi_yN_z$ to the other films previously discussed in this study.

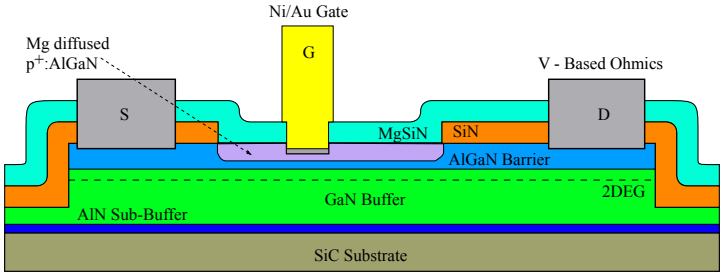

Figure 7.7: Proposed doped field plate device incorporating both Si_yN_z and $Mg_xSi_yN_z$ dielectrics as well as a doped field plate region.

would only allow Mg to diffuse into the AlGaN in the vicinity of the gate region, leaving the regions near the source and gate passivated by Si_yN_z which would provide for lower sheet resistivities there. A proposed device of this type is depicted in Figure 7.7. Careful optimization of the parameters in these processes have the potential to significantly increase the breadown voltage, efficiency, and output power density of AlGaN/GaN HEMTs at increasingly higher frequencies without the use of metal field plates.

APPENDIX A

ALGAN/GAN HEMT FABRICATION PROCESSING PARAMETERS

A.1 Introduction

This section provides additional processing notes for specific processing steps mentioned in Chapter 4 of this document. All processing was performed at the Cornell Nanoscale Facility at Cornell University in Ithaca, NY.

A.2 Plasma Etch Processes

A.2.1 Yield Engineering Systems (YES) Asher

Resist Descum Process (#3)

Chamber pressure: 350 mTorr

O_2 Flow rate: 100 sccm

Chuck temperature: 80°C

RF Power: 100 W

Post Ohmic Lift-off Clean Process (#12)

Chamber pressure: 350 mTorr

O_2 Flow rate: 100 sccm

Chuck temperature: 200°C

RF Power: 1000 W

A.2.2 Aura 1000 Resist Ashing Etcher

Mesa Clean Process (#03F)

Chamber pressure: 2 Torr

O_2 Flow rate: 5000 sccm

Process temperature: 250°C

RF Power: 2000 W

A.2.3 PlasmaTherm 770 ICP-RIE Etcher

Mesa Etch Process (brown.bch)

Chamber pressure: 25 mTorr

Cl_2 flow rate: 20 sccm

BCl_3 flow rate: 8 sccm

Ar flow rate: 5 sccm

ICP power: 400 W

RIE power: 50 W

DC bias: 100 V

Dielectric Passivation Etch Process (brown2.bch)

Chamber pressure: 25 mTorr

SF_6 flow rate: 10 sccm

BCl_3 flow rate: 10 sccm

Ar flow rate: 5 sccm

ICP power: 500 W

RIE power: 100 W

DC bias: 115 V

SF_6/Ar Dielectric Etch Process (rjbsf6ar.bch)

Chamber pressure: 15 mTorr

SF_6 flow rate: 45 sccm

Ar flow rate: 5 sccm

ICP power: 150 W

RIE power: 75 W

DC bias: 100 V

A.2.4 Oxford Plasmalab 80 RIE Etcher

Evaporated SiO_2 Definition / Source and Drain Dielectric Etch

Chamber pressure: 55 mTorr

CHF_3 flow rate: 50 sccm

O_2 flow rate: 5 sccm

RIE power: 150 W

DC bias: 60 V

Amorphous Carbon Definition / Antireflection Layer Clear

Chamber pressure: 60 mTorr

O_2 flow rate: 50 sccm

RIE power: 150 W

DC bias: 45 V

A.3 Deposition Processes

A.3.1 Ion and Plasma Equipment (IPE) 2000 PECVD System

Amorphous Carbon Deposition

Chamber pressure: 450 mTorr

Chuck temperature: 150°C

CH_4 flow rate: 54 sccm

RIE power: 50 W (5% total power)

Silicon Nitride Deposition

Chamber pressure: 550 mTorr

Chuck temperature: 300°C

NH_3 flow rate: 60 sccm

SiH_4 flow rate: 18 sccm

RIE power: 50 W (5% total power)

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